

Digitally Controlled Trimmable Resistor

DESIGN DOCUMENT

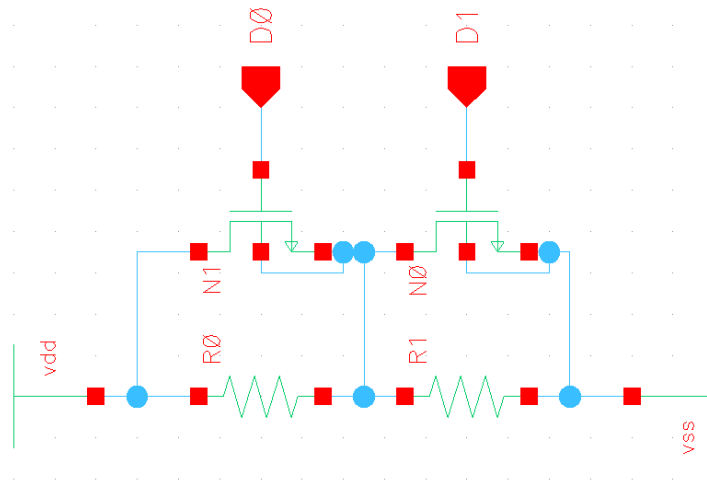


Figure 1

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Executive Summary

Development Standards & Practices Used

- IEEE - Follow all IEEE codes of ethics and designing standards for integrated circuits.
- Virtuoso - Follow all virtuoso rules when designing the circuit schematic, layout and running simulation.
- TSMC Process Parameters - Follow process parameters provided by TSMC to make the circuit simulatable and manufacturable.
- Design Flow - Follow a design flow methodology presented in class in order to organize our projects progress. This includes Empathy, Define, Ideate, Prototype, and Test.
- MATLAB - Use good coding practices for maintaining usability and readability. Comment all code for clarity.

Summary of Requirements

- Make a device in .18u CMOS process with adjustable resistance
- Make the resistor high resolution with a 1% trim
- Size the layout of the circuit to compete with trimmable resistors currently available
- Minimize temperature dependencies within the design
- Manage process variations issues within the design and layout of the circuit
- Be able to adjust the resistance with a discrete input

Applicable Courses from Iowa State University Curriculum

- EE 201 - This course provides the background on relevant passive components that will be used in our design. It also gives us some of the mathematical tools necessary to work with analyzing passive components.
- EE 230- This course covers operational amplifiers. These devices will be used in our simulations.
- EE 330- Gives background knowledge on semiconductor devices like MOSFETs which is a dominant component for the operation of a digitally

- controllable circuit. This course also teaches us how to do physical layout of an IC.
- CPR E 281- Gives us the digital background for our digitally controlled trimmable resistor. Encoders, decoders, and other digital logic that we might use in our design was learned here.
 - MATH 267- Differential equations gives us many analysis techniques that are applicable with circuitry. This course is a foundation for the development of our trimmable resistor.
 - EE 332- Physics of semiconductors. This course goes into depth on the characteristics of the materials used to create the switches (mosfets) used in this project design.
 - LIB 160- This course provides a solid understanding of information literacy and the research process. LIB 160 allowed us to discover many web resources for our research via the use of library discovery tools. These tools will be extremely useful since most of our project is research.
 - EE 394- This course helped us to discover the importance of ethics in everything we do.
 - ENGL 314- While making our way through this project, we will need to do a lot of documentation. English 314 taught us how to successfully communicate technical information to a specific target audience.

New Skills/Knowledge acquired that was not taught in courses

- Research - Although we discussed resources for research in LIB 160, we have not actually had any courses that focused on pure research. Senior design has given us the opportunity to learn how to research with a particular technical goal in mind.
- Website management- We are a group of mostly electrical engineers with the exception of one computer engineer. This being the case, we have not really dealt with using/designing/managing websites up until this point.
- Several tools and resources- We have learned about the existence of different tools and resources that have been helpful for our progress so far and will continue to be helpful down the road.

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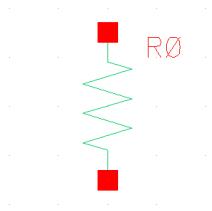
Definitions:

EE	- Electrical Engineering
CPR E	- Computer Engineering
IC	- Integrated Circuit
MOSFET	- Metal Oxide Semiconductor Field Effect Transistor
PCB	- Printed Circuit Board
CMOS	- Complementary Metal Oxide Semiconductor
.18u	- 18 Micron CMOS process
PPM	- Parts Per Million
TCR	- Temperature Coefficient of Resistance
TCV	- Temperature Coefficient of Voltage
Cadence	- Company that created Virtuoso
Virtuoso	- Circuit schematic design software
Spectre	- Simulation environment within Virtuoso
NMOS	- N-type Channel MOSFET
Unit Cell	- Circuit design used as a building block for other circuits

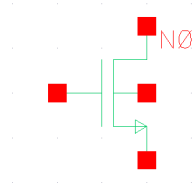
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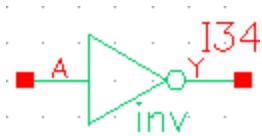
Symbols:



Resistor



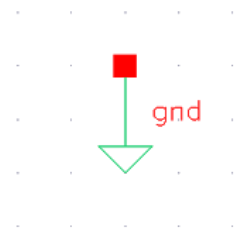
NMOS transistor



Inverter



Voltage Source



Ground

1 Introduction

1.1 ACKNOWLEDGEMENT

A big thanks to Randy Geiger for his time and technical advice throughout our project.

1.2 PROBLEM AND PROJECT STATEMENT

Currently in industry, there is a need to modify resistance values for resistors that have been implemented into a working circuit design. There is a way to trim resistors by laser cutting the resistor film to finely set the desired resistance value. This has the disadvantage of being expensive as well as impossible to do once the IC has been packaged. Also, it is a one-time process that only allows the resistor to be trimmed once. Another solution is with a digital potentiometer using a series, parallel, or ladder resistor structures. This digital solution has low-resolution trimming capabilities with either poor temperature coefficients or physically large components.

This project aims to create a high-resolution digitally trimmable resistor that will fix many of the current solutions. This device will be able to set different resistor values using a digital input that can be finely tuned to different resistance values within a set range. The focus of the project is to improve an architecture based on resistors and switches; the goal is to construct a digitally trimmable resistor that has a high resolution with good temperature coefficients.

1.3 OPERATIONAL ENVIRONMENT

There are no specific plans for the operational environment of the IC. Conditions such as dust and rain could be mitigated through a device enclosure. Since one of the goals is to minimize the temperature dependencies on the MOSFETs and resistors, extreme temperatures should not be an issue. As such, the design can be utilized in most conditions.

1.4 REQUIREMENTS

This device requires a resistor that can be repeatedly trimmed over many iterations. The resistor should be modifiable by around 1% divided up into smaller binary step sizes. This device will require the use of a decoder to set the digital inputs necessary to select a resistance value. It will require a PCB to interface with the device. Lastly, temperature dependencies must be minimized.

1.5 INTENDED USERS AND USES

A digitally controlled trimmable resistor could be used in applications that require an initial calibration, where certain parameters need to be altered. One example is in an amplifier where the gain needs to be precisely set. Another example of where a trimmable resistor is used is in a cardiac pacemaker. Electrical parameters in this type of environment need to operate within small margins.

1.6 ASSUMPTIONS AND LIMITATIONS

Assumptions:

Resistors and MOSFET devices are very temperature dependent by nature. In addition, process variations will exist with all circuits once manufactured. Only resistors and MOSFETS will be used, and the circuit should be re-trimmable many times.

Limitations:

The overall size of the resistors and the switches will need to be small. The trimming should be binary weighted where the total trim resistance adds up to 1%. The temperature coefficient of the whole structure should ideally be equal to the resistors temperature coefficient.

1.7 EXPECTED END PRODUCT AND DELIVERABLES

The expected deliverable is a new method for a digitally controlled trimmable resistor, as opposed to what is currently being used. The design will be within the limitations provided. After coming up with a new approach and the appropriate measurements, the circuit would be simulated using the .18u CMOS process. The end goal is to get a simulation of a device that will meet the constraints set by the client. No physical deliverable is required.

2. Specifications and Analysis

2.1 PROPOSED APPROACH

Current Progress:

We have successfully completed the requirement of the project upon successful simulations of the voltage divider and the ladder structure. Both structures are 4-bit and binary weighted, where the max trim is 1% of the overall circuit resistance. In addition, the voltage divider takes up less area than the reference design known as the ladder structure and the voltage divider had better TCV performance than the reference design.

Approaches:

The approach followed for this research project started off with extensive research in applicable areas of integrated circuits. Gathering and evaluating previous work and literature to learn about current industry standards and designs. After researching various current methods of trimming a resistor, our team brainstormed potential designs and later simulated them. Simulations were run using a realistic and accurate environment to test various parameters of interest like TCV and TCR. Simulator parameters like Abstol were modified to produce very accurate simulation data. Evaluation of the ability to meet requirements specified were followed on specific simulation. After the evaluations were made, the various designs were compared to one another.

Standards:

Relevancy to standards falls heavily under the IEEE code of ethics. As research is conducted on current industry practices, credit will be given according to contributions in the design where applicable. Another standard for this project is the CMOS process that is selected for circuits that are designed. The .18 CMOS process will be used as a constant process for all of the designs. Since the end goal is a simulated circuit, other standards are not anticipated as relevant to this project.

2.2 DESIGN ANALYSIS

Initial structures tested include the series resistor design, and the parallel resistor structure. These approaches have been modeled in Virtuoso and tested in order to examine the trimming resolution and temperature coefficient properties. Examples include the series design which has a major flaw due to the current path flowing through MOSFETs. When current flows through the MOSFET, temperature variables affect the performance. Another example is the parallel design. The

parallel designs' flaw shows up in the physical size of the IC due to the resistors being in parallel. Overall the analysis should show the ability of the design's resolution capabilities and temperature stability.

2.3 DEVELOPMENT PROCESS

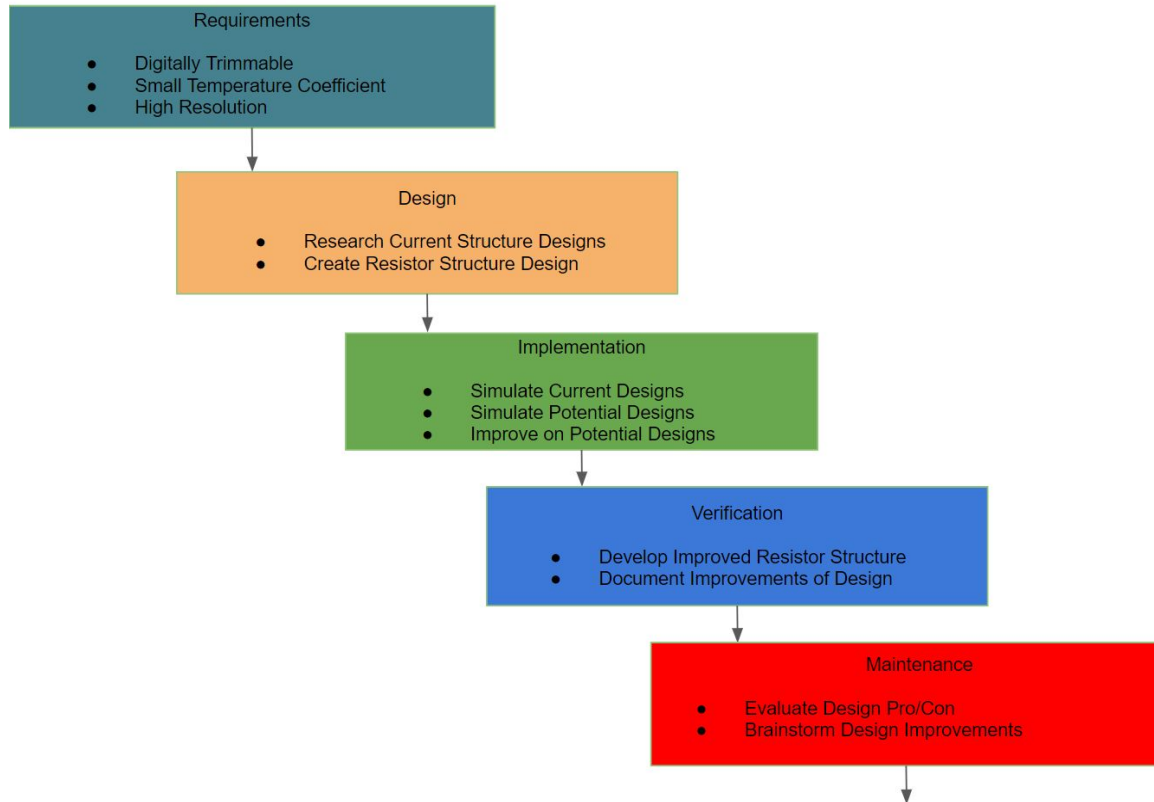


Figure 2.3.1

For this project, a waterfall development process was being followed. The requirements phase was for spending time researching design requirements. Next, the design phase was used for researching current solutions on the market and using those ideas to brainstorm new structures. Once completed, the brainstormed designs went into the implementation phase where they were simulated and tweaked up until their performance met the requirements of the project. The performance was verified with our advisor to make sure the project goals were met. Then in the maintenance phase is where the pro's and con's of the structures were determined.

2.4 CONCEPTUAL SKETCH

Series Structure:

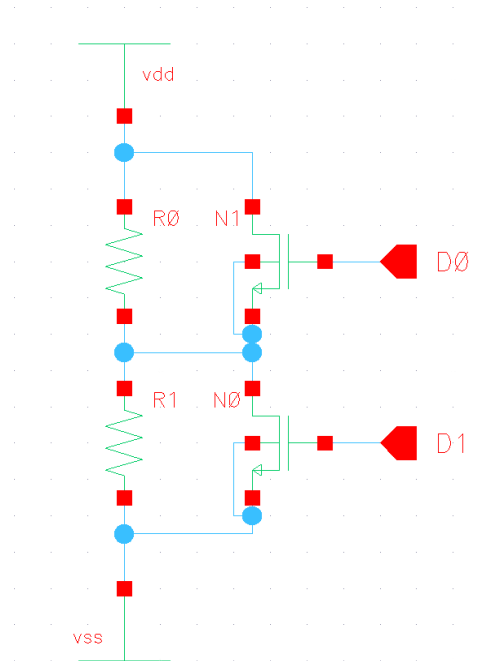


Figure 2.4.1

The first trimmable resistor design created was a series structure where resistors are put in series out to the n^{th} bit, and then switches are put in parallel to a respective resistor. With an encoder, the gates on the switches can be set to high or low resulting in the switches opening or closing. When a switch is closed, ideally, an electrical short beside the resistor will occur which essentially will allow current to completely bypass the resistor. This allows for trimming of the overall resistor unit cell. When driving current through a MOSFET, temperature variations are unfortunately introduced. This is a big performance issue due to breaking the voltage divider ratio by introducing new temperature dependencies.

Parallel Structure:

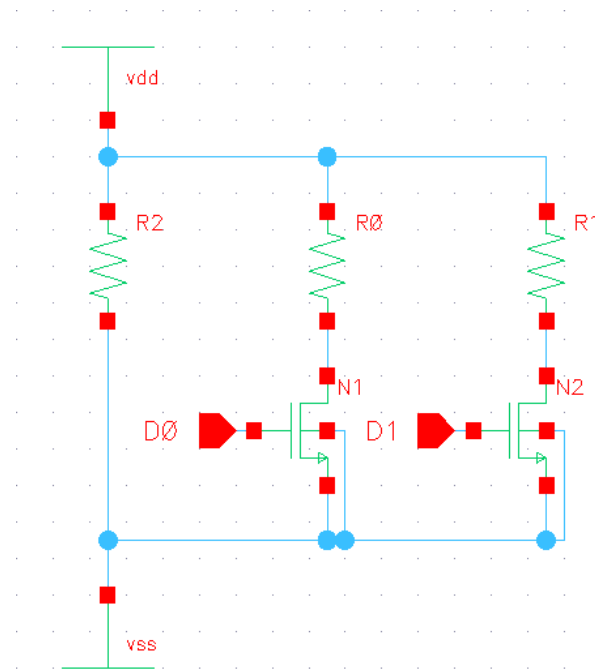


Figure 2.4.2

Another approach discussed was positioning the resistors in parallel which would result in the MOSFETS in series with the resistors. When a switch is open, current does not flow through the respective path; therefore, that path does not interact with the performance of the unit cell. When a switch is closed, current flows through the resistor which in turn will affect the performance of the unit cell. Unfortunately resistors in parallel are added by taking the inverse of the resistor value, so with a parallel resistor design the resistors become exponentially large. This negatively impacts the physical size of the design.

Matrix Structure:

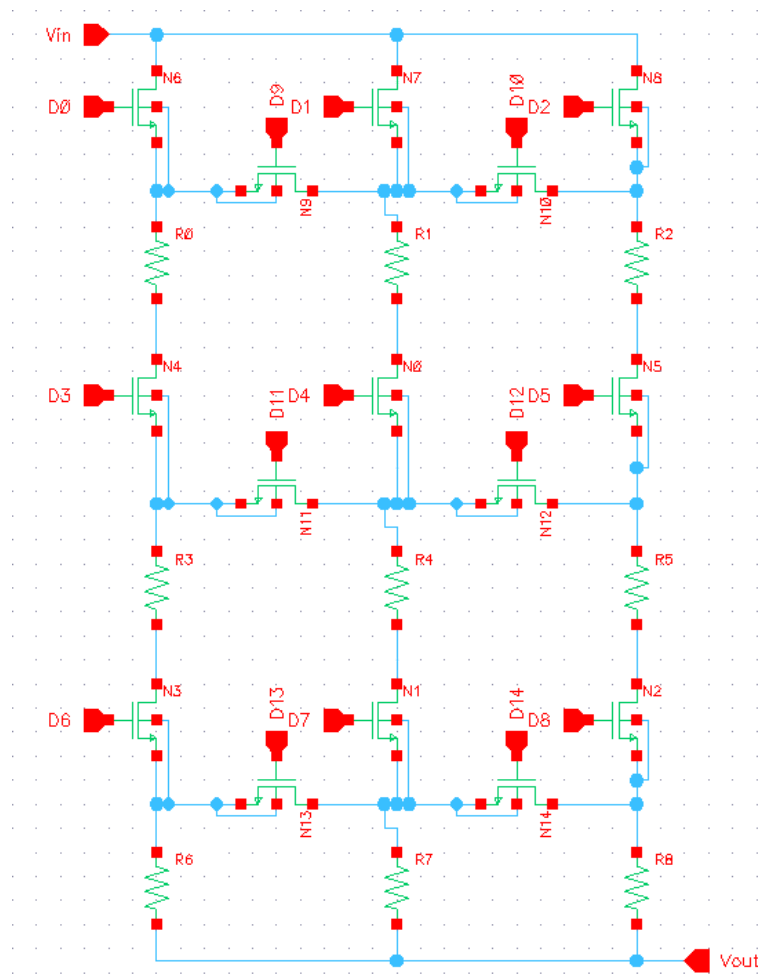


Figure 2.4.3

After looking at a series and parallel approach to trimming a resistor, the idea of combining them was proposed. By combining the two designs previously discussed we hope to mitigate the negative effects each of the designs have. Figure 2.4.3 shows a matrix of resistors that have resistors in series and parallel. Then by using switches between the paths we are able to control the flow of current through the matrix of resistors. This then results in a trimmable resistor with the negative effects being mitigated in the process.

Ladder Structure:

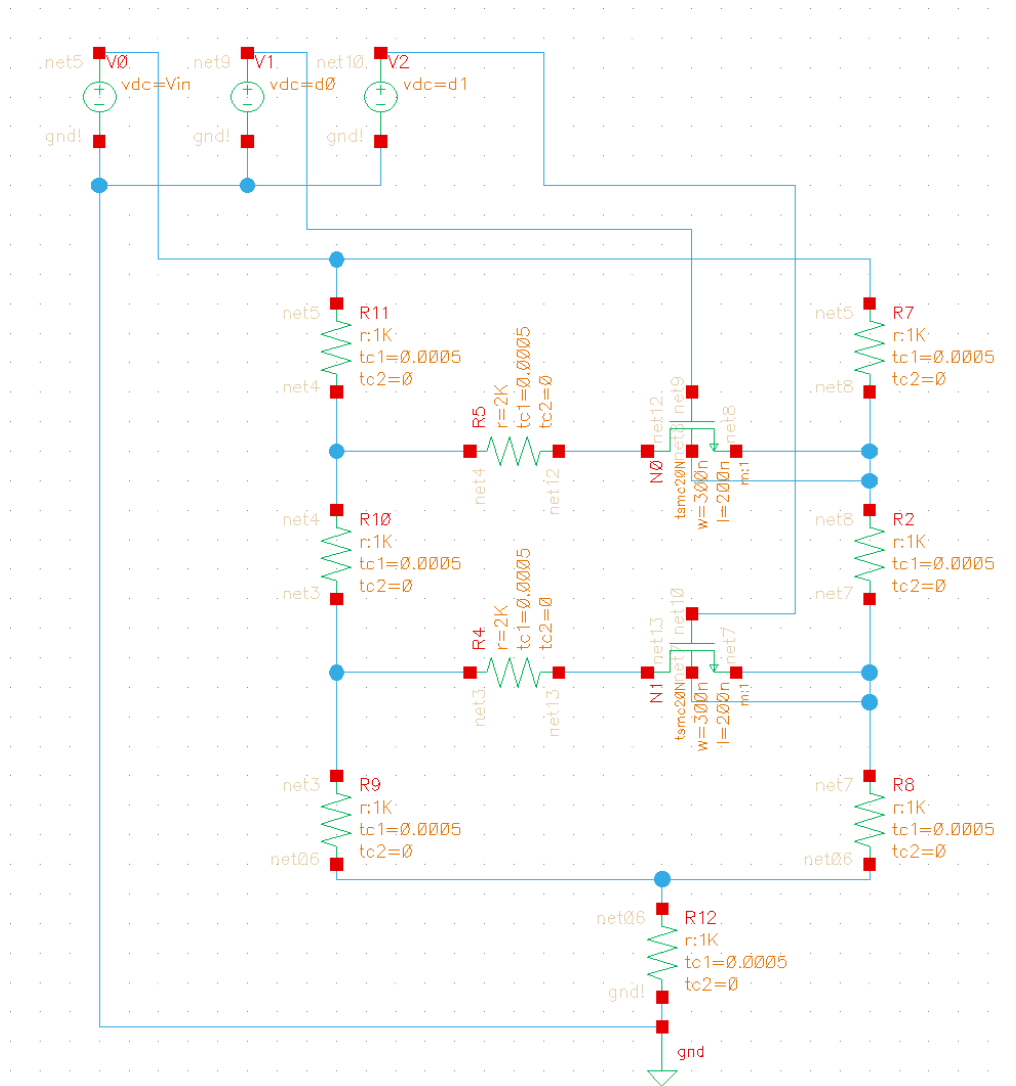


Figure 2.4.4

A design that has been given to use by our advisor was the ladder structure. This design is advantageous because of its ability to avoid TCR effects. The idea of this design is to ensure that the current avoids flowing through the MOSFET devices. Both the on/off states of the switch will ideally have the same TCR effects.

Truss Structure:

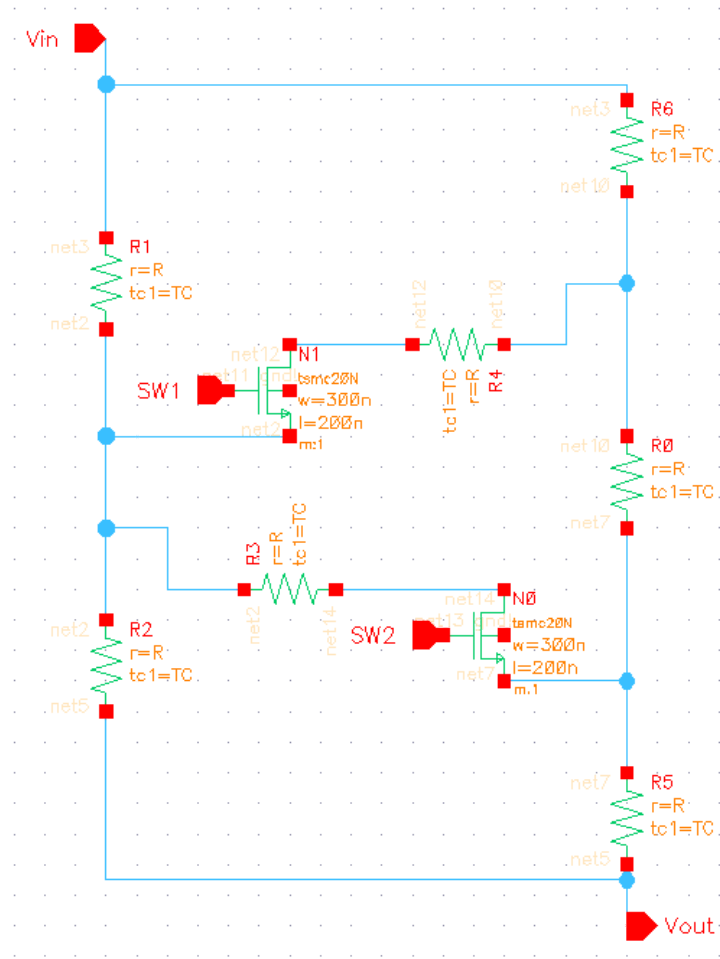


Figure 2.4.5

The truss structure shown in Figure 2.4.5 was inspired by the ladder structure use of current driving legs which would result in a great TCR performance. The difference however from the ladder structure is how the trimming switches are orientated.

Voltage Divider Structure:

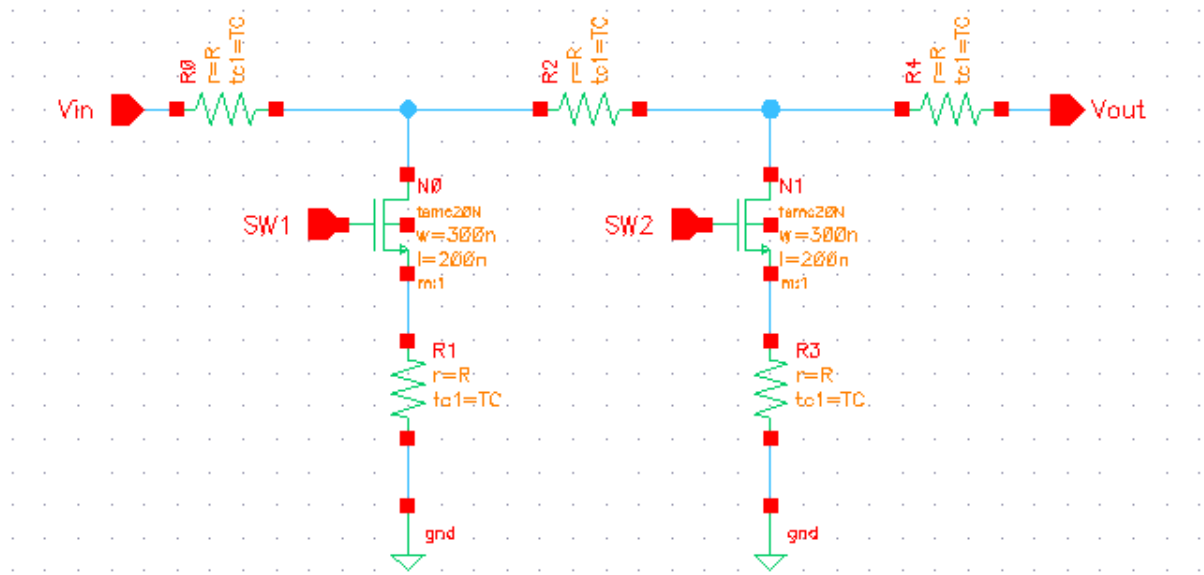


Figure 2.4.6

One of the most promising designs initially was the voltage divider structure. This structure takes the traditional voltage divider and expands it to 4 bits by placing switches before the vertical resistors. The design was advantageous due to its ease of implementation. It also has resistors placed in good symmetry to balance out temperature effects.

T-Branch Structure:

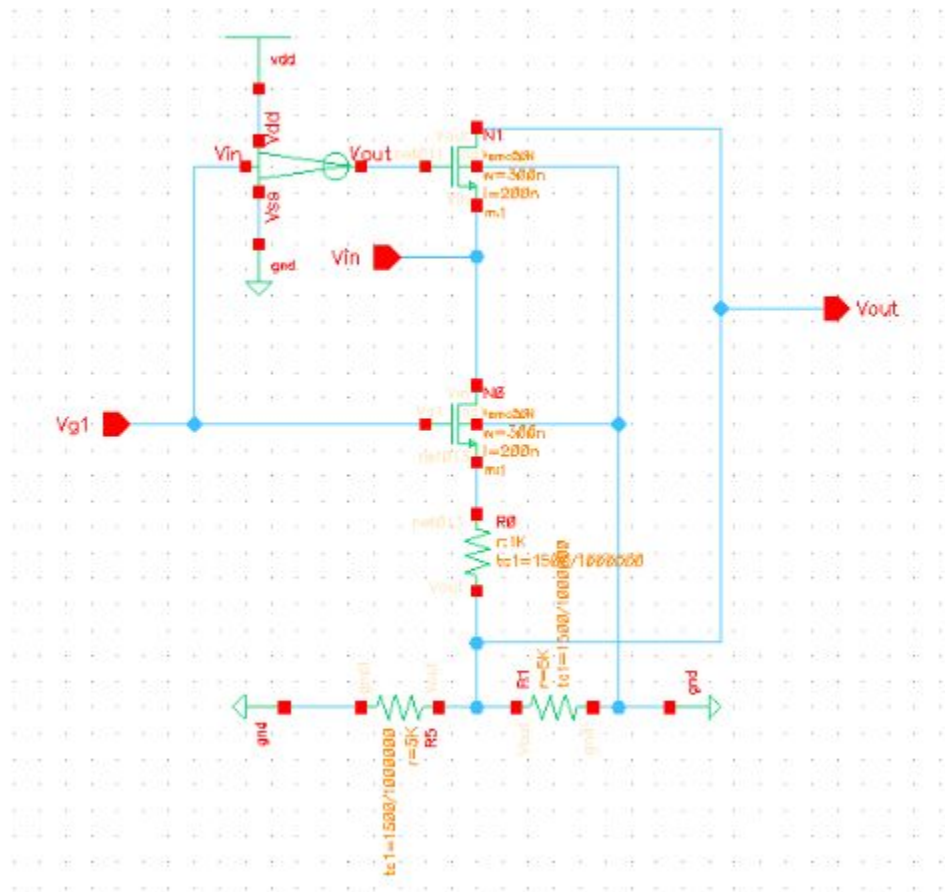


Figure 2.4.7

The idea behind this structure was similar to that of the voltage divider. The inverter would control the switch at the top and allow a bypass directly to the output if the bottom switch was off. This would emulate the idea of an open switch. If the middle is closed (in an on state), then the circuit would act as a voltage divider with 2 resistors on the bottom for more geometric symmetry.

3. Statement of Work

3.1 PREVIOUS WORK AND LITERATURE

The first work of relevant literature for information on this project's topics is “The Art of Analog Layout”, by Alan Hastings [1]. A second piece of literature relevant to the work on this project is the textbook Analog Integrated Circuit Design by T. C. Carusone, K. W. Martin, and D. Johnsby [2]. Another good resource on this topic is the book Microelectronic Circuits by A. S. Sedra and K. C. Smith [3].

The previous work of this type of trimming has been used in many applications requiring the ability to precisely trim a chip after manufacturing where laser trimming is not available. Documentation of previous work includes a patent by Cardiac Pacemakers Inc, where digitally trimmable resistors were used for bandgap voltage reference [4]. This method used a series resistor structure which has been simulated as one of our reference designs. This design has the shortcoming of having a poor temperature coefficient due to the large amount of current flowing through the switches.

Another popular method for trimmable resistors is the ladder structure. In a patent by Jimmy R. Naylor, a $R/2R$ Ladder structure of resistors was implemented in order to create a new method for digital to analog converters[5]. This ladder structure is a promising resistor structure because of its improvement on both the series and parallel approaches. This is the primary structure that our project will be focusing on improving.

Other methods of trimmable resistors include the patented dual thin film precision resistance trimming by STMicroelectronics Inc [6]. This design implements a heater on the IC that can precisely control the temperature of the resistors. This utilizes the temperature coefficient properties to modify the resistance values and achieve a fine resistor trim. A drawback of using an on-chip heater is the amount of space that will be required to do so. Space is part of the project requirement and therefore the heater is not something that can be utilized. It also takes a lot of power to use an on-chip heater, which is another drawback of this approach.

To focus on the digital trim, other sources have been used as resources to further improve the trimming designs. Utilizing the textbook and lecture material from our academic advisor, Dr. Geiger was a crucial part as a starting point in TCR optimization [7]. One paper from the Journal of Applied Physics, titled “The electrical properties of polycrystalline silicon films” allowed us to get a more in depth correlation to the temperature characteristics of the resistors in the process selected [7].

3.2 TECHNOLOGY CONSIDERATIONS

This project relies heavily on MOSFET technology as switches in the trimmable resistor. Current MOSFET technologies do have a few weaknesses, however. The major one is the non-linearity performance due to temperature effects. If the switches were ideal, then the performance degradation caused by temperature effects would not be an issue. Unfortunately, these effects are a genuine issue throughout this project, but there are a few solutions to this issue. One such solution is to limit the amount of current flowing through the MOSFET to reduce the adverse effects. The tradeoff of doing this will be the need for more switches in the circuit. Solutions to the temperature effects could result in a tradeoff. The pros and cons of each solution will need evaluating to ensure that the solution is a valid one.

In addition, there will be a tradeoff with the physical size of the circuit and the accuracy. As a focus on accuracy becomes a dominant player in our design, the circuit will become much larger; therefore, our team will need to define what an acceptable physical size of the circuit is and then pack as much accuracy into the circuit given the circuit size limitation.

3.3 TASK DECOMPOSITION

In order to successfully complete the digitally programmable trimmable resistor, our team broke up the project into multiple tasks.

- 1) Meet with our advisor to discuss technical goals, progress, and to make changes as needed.
- 2) Research existing designs and review our fundamentals.
- 3) Ideate and discuss ideas our team brainstormed.
- 4) Simulate reference design and acquire temperature coefficient.
- 5) Simulate our designs and compare them to the reference design performance.
- 6) Pick the most promising design based on performance characteristics and hone it into a finished product.
- 7) Prepare presentation and documentation.

Above were the tasks that helped our team stay on track to finishing the project.

3.4 POSSIBLE RISKS AND RISK MANAGEMENT

One major hindrance to the success of our project was access to the virtuoso software needed in order to design and simulate potential circuits. Some reasons that might make it difficult to access Virtuoso would be remote desktop issues, vpn issues and lab room closures. Additionally, there may be times when team members will have issues with their internet access.

Another roadblock that came up was simulation issues due to lack of knowledge on the proper way to perform simulations within Virtuoso. Our team needs to rely heavily on the simulation results in order to determine the performance of circuit designs, but if simulation issues present themselves, then our team will need to remove this road block before any more progress can be made.

Lastly, when it comes to circuit design, there are a lot of nuances and rules that need to be understood in order to successfully get a circuit to behave properly. During the project, our team's knowledge on the general operations and behavior of circuits was adequate for designing and simulating but if it was not, then some new risks would have appeared.

3.5 PROJECT PROPOSED MILESTONES AND EVALUATION CRITERIA

Over the course of our projects progress, there are a few milestones that will need to be hit. Below lists a few of the milestones that our team will work towards reaching.

- 1) Measure the temperature coefficient of a resistor.
- 2) Measure the temperature coefficient of a MOSFET.
- 3) Simulate the ladder structure successfully with a thermometer coded trim
- 4) Simulate the ladder structure successfully with a binary trim
- 5) Simulate the structure designs successfully with a thermometer coded trim
- 6) Simulate the structure designs successfully with a binary trim
- 7) Measure the temperature coefficient of the ladder structure
- 8) Measure the temperature coefficient of the structure designs
- 9) Pick the best performing circuit to present as our solution to the problem statement.

By performing well established simulations, we should be able to confirm proper operation of the design. If there are any questions regarding the accuracy of any results, they can be directed to the faculty advisor. The faculty advisor is an expert in the area and should be able to provide us with meaningful and reliable guidance.

3.6 PROJECT TRACKING PROCEDURES

Google Drive has been the primary source of project tracking since we are unaware of any Virtuoso collaboration tools. Google Drive allows us to share created content with each other so that it can be improved upon. It also documents any completed assignments and important resources. Other methods of project tracking include recording online meetings with Google Meet for documenting project checklist items, documenting updates within Google Slides for tracking presentable progress, and Microsoft Sharepoint for documenting data collection and calculations.

3.7 EXPECTED RESULTS AND VALIDATION

The desired outcome is a digitally controllable trimmable resistor design. This trimmable resistor will need to have high accuracy and resolution, as well as low temperature dependencies in order to compete with current designs in the market.

For high level verification of the voltage divider structure our team worked to tune it to match nearly ideal or ideal performance.

4. Project Timeline, Estimated Resources, and Challenges

4.1 PROJECT TIMELINE

sddec20-o8 Gantt chart



Figure 4.1.1

The work is split up between two semesters, using the first semester mostly for research, administration, and ideation. The first half lays a proper groundwork leading into the second half of the project. The focus in the second half is in choosing specific designs that show promise and refining them until they meet the project requirements. The focus then shifts to preparing documentation and running proper tests to confirm everything is accurate. Finally, we present our findings to an industry panel along with the documentation that was developed, proving that the design meets the project requirements.

4.2 FEASIBILITY ASSESSMENT

This project consisted of researching current methodologies of resistor trimming technologies. The goal was to improve upon current technologies and develop a new resistor concept that garners interest as a useful product in the electronics community. In particular, the product will be a high-resolution digitally trimmable resistor that has minimized temperature dependencies. The challenges associated with this project were mostly that of the feasibility variety. Research and development in this area required specialization of the topic which we had to learn as we progressed on the project. Another challenge encountered were simulation results that were not quite aligned with reality.

4.3 PERSONNEL EFFORT REQUIREMENTS

Task	Time/Person
Administrative	20 hrs
Research	30 hrs
Ideate	20 hrs
Simulate	30 hrs
Development	50 hrs
Documentation/Presentation	30 hrs

Table 4.3.1

4.4 OTHER RESOURCE REQUIREMENTS

The materials needed for this project were as follows:

- Computers for each team member
- Internet connection for each team member
- Communication software
- Simulation software

All of the materials were accessible to each member with no extra associated costs.

4.5 FINANCIAL REQUIREMENTS

There were no financial resources required to conduct this project. Everything was digitally designed and simulated. All resources for this project have been provided by Iowa State University at no cost.

5. Testing and Implementation

Fundamentally the project is made up of 3 parts:

- Research
- Ideation
- Testing

The first step was researching concepts and ideas that can be used in the designs. The next step is to come up with circuits that encompass the research results to meet the goal. Then, the circuits are tested to ensure that the test results are as expected and meet the required goals. Testing is a key component as it allows the designer to evaluate their ideas. This gives them the ability to choose a final design that has the best performance relative to the goal. Because testing is so important, it is important that all of the tests are true and complete. Validity of a circuit as a product cannot be determined if the test that is used to validate it is wrong or inadequate.

All of the design work is done in Cadence Virtuoso, and the testing is done through Cadence Spectre within Virtuoso as well as through MATLAB using a custom script. For each circuit design, the following tests are needed:

- Temperature coefficient
- Scalability (can we go from a 1-cell design to an n-cell design)
- Resolution of the trimmable resistor
- Accuracy of the trimmable resistor
- Monotonicity of the trimmable resistor
- Reproducibility of expected results (can we re-trim the device over and over again)

The individual items to be tested are as follows:

- Resistor
- NMOS transistors

The individual designs above will be tested to ensure the simulation environment is behaving correctly and the component parameters are correct.

To determine the resolution and the range of the trimmable resistor, a sweep through all possible state combinations of the switches will be performed. To test the scalability of the design, one unit cell will be created and tested in a test bench to ensure proper functionality. To check the expansion of the design, more unit cells will be cascaded into the test bench and make sure the functionality is still achieved. Reproducibility of the device will be determined by repeatedly running

tests and verifying that the resulting output is the same as the first test run (within a specified tolerance). Finally, to check the temperature coefficient of the design, a dc sweep ranging from 0 to 100 degrees celsius will be created. The input voltage and input current will be plotted afterwards. Once plotted, Microsoft Excel will be used to calculate the temperature coefficient values per sweep step.

The anticipated test results for the temperature coefficient of the designed circuit is ideally zero. A temperature coefficient of zero may not be possible, so the goal will be to get it as close to zero as possible. Scalability of the circuit will be determined by whether or not the goal has been met. It is expected that an individual cell should function such that adding more cells to it will meet the goal of the overall circuit. If the cells cannot be cascaded until the goal is met, the circuit is not scalable. Resolution of the resistor needs to be high. The goal is a total trim of $\pm 1\%$. Reproducibility will ideally be infinite, but there will be physical limitations when the circuit is brought into the real world. Simulation results of the circuit are expected to be reproducible 100 times once it passes initial testing for other requirements.

The implementation of this device is beyond the scope of this project. The potential implementation of this device includes applications in many aspects of IC products. Some examples of implementation include but are not limited to digital to analog converters known as DAC's, compensation for manufacturing errors in resistor components, and digital potentiometers known as digiPOTs. These devices themselves also have a wide range of applications. For example, digiPOTs are used for adjustable gain amplifiers, sensor trimming and calibration, programmable power supplies, controller circuits, or can be used to control current flow as a rheostat.

5.1 INTERFACE SPECIFICATIONS

All testing interface tools will come from Cadence Virtuoso, the Cadence Spectre simulation environment, and custom MATLAB scripts.

5.2 HARDWARE AND SOFTWARE

All testing and simulating is done using custom MATLAB scripts, Virtuoso, and the Spectre toolkit included in Virtuoso. Many tests are performed using dc sweeps across temperature. This is useful because it will perform the simulation over a range which would take a lot of time by hand to do. Microsoft Excel is used to break down the plots generated by Virtuoso to better analyze the results.

5.3 FUNCTIONAL TESTING

Unit Tests:

Both the resistor and the MOSFET components will be tested to ensure the simulation environment is behaving correctly and the component parameters are correct.

Integration Tests:

Unit cells will be tested in a Virtuoso test bench to make sure the behavior of the unit cell is as expected.

System Tests:

After testing all the unit cells, the unit cells will be combined to increase the resolution and range of the resistor. It will be tested using a parametric analysis across all input variables to generate a plot. The plot will be analyzed to ensure proper behavior was observed.

Acceptance Tests:

The overall acceptance test will be completed once the completed circuit is made. Then the test results will be compared to the reference design to determine if any performance characteristics have improved.

5.4 NON-FUNCTIONAL TESTING

Testing for Performance:

The trimmable resistor will be tested for performance by cycling all digital input combinations to ensure the trimmable functionality works. Then the trimmability accuracy will be tested by attempting to trim the resistor to an exact value.

Testing for Security:

This is not applicable for a trimmable resistor type project.

Testing for Usability:

The circuit's usability will be tested by making a few test bench applications where a trimmable resistor may be applied. In addition the input voltage range of the circuit will be comparable to other similar trimmable resistors currently on the market .

Testing for Compatibility:

The circuit will be capable of accepting a wide variety of input signals thus making it compatible with most users' applications. To test for this, the circuit will be tested in a test bench test environment.

5.5 PROCESS

Various simulations will be carried out to ensure the components are being used in their appropriate environment and that the resolution is high enough, this would require some trial and error. Microsoft Excel has the ability to import the results from Spectre and allows a better analysis of the data.

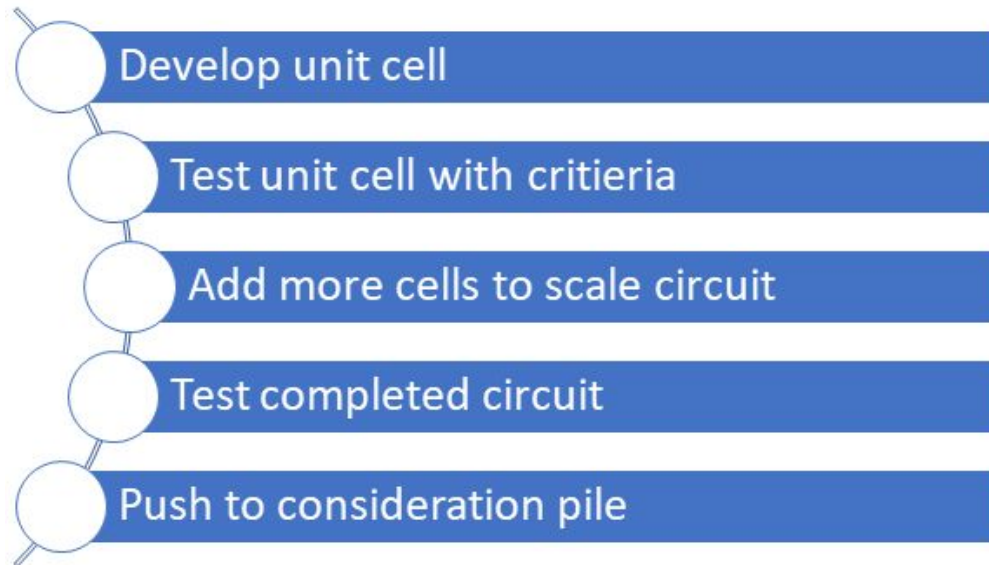


Figure 5.5.1

The initial test performed was to get a basic series trimmable resistor circuit (figure 2.4.1) to run that way we could have this reference circuit to compare with our final product.

During the testing phase, there was one issue that took the front stage; how Virtuoso handles temperature coefficients. Due to the nature of integrated circuits, getting the correct behavior for temperature characteristics is key. To overcome this issue, research in polysilicon temperature characteristics resulted in finding polysilicon conductivity.

The first approach we took was having a constant TCR. We simulated our circuit with a TCR of 500 ppm/°C which we found from Dr. Geiger's lecture notes. The results from this simulation gave us a linear equation for the TCR of resistance. We realized that our equation for TCR was different from Cadence's equation. This is because Cadence uses an equation that takes a nominal resistance value as a parameter, while our equation uses the temperature value at the temperature where the TCR is being measured.

We realized that the real TCR needed to be discovered through the material properties of polysilicon. We arrived at the idea that the inverse of conductivity is the resistivity. From that discovery, the temperature coefficient equation can be derived from the derivative of resistivity with respect to temperature divided by the resistivity. In addition to the temperature dependence of the equation, the

TCR varies depending on the material properties of the polysilicon. Depending on the carrier concentration of the polysilicon, the energy barrier will change resulting in a change in the TCR. An equation was tested in a simple voltage source resistor circuit, and the result is shown in figure 5.6.1. There were many iterations of equations tested with different parameters. A final resistor material and TCR parameter was found that can be used for our designs. With our newfound knowledge, all the future simulations of circuit designs can be run with the proper resistor parameters for our fabrication process.

There are various standardized testing components and operating parameters that were modified over the course of the project that are listed and explained in the results section of Testing and Implementation.

Tests for TCV were conducted by running a dc temperature sweep with a parametric analysis of bit combinations in Cadence Spectre to analyze the temperature characteristics for each design.

Tests for trim levels were conducted using the custom MATLAB script which outputs trim values for each bit combination. This outputs information about the trim value trend over each bit combination, accuracy and error of each bit combination, and total trim capabilities.

The next stage of testing was started within Virtuoso to scale up resistor structure designs to 2-bit structures followed by implementing a binary weight to the structures. We decided to focus on three main resistor structures for testing and analysis. The truss structure, the voltage divider structure, and the ladder structure were selected. Furthermore, testing was conducted within Virtuoso to optimize the trimming values, total resistance size, and TCV for our selected designs.

The testing process progressed into scaling up both the voltage divider structure and the ladder structure into 4-bit binary weighted designs for further testing. These designs were tested similar to the 2-bit binary weighted versions with the added analysis of scalability for the potential of increased trimming capabilities or improved resolution capabilities.

5.6 RESULTS

Results from the analysis of TCR variability in Virtuoso

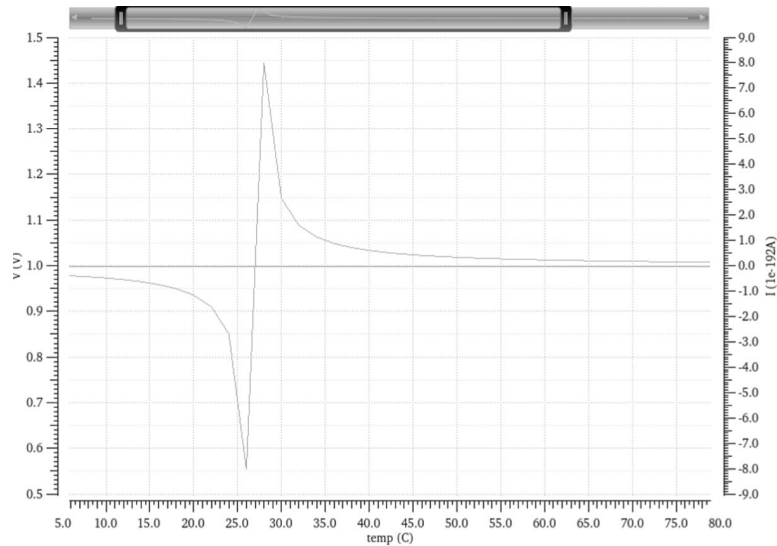


Figure 5.6.1

Results from many iterations of the initial tests showed the need for reconfiguration of the standardized operating parameters for further testing. We realized that some testing parameters were not completely standardized and did not have a compatible comparison environment. The most important change we made to the standardized testing was to implement 2-bit structures that incrementally increased up to a total of 1% trim amount either up or down. We also changed one of our tests to compare to the temperature coefficient of voltage, TCV, instead of TCR. Another modification was to the trimmable resistor parameter. We decided to trim a 10 kOhm resistor. We changed the resistor components to 1500 ppm/°C and maintained the nmos components at 300n x 200n.

Comparison between Ladder and Voltage Divider Structures:

The first comparison between the two competing structures is the trim level. This comparison provides data for the trimming capabilities at each bit combination. The evaluation parameters used to determine the best performing structure was the linearity, accuracy, and monotonicity of the trim levels.

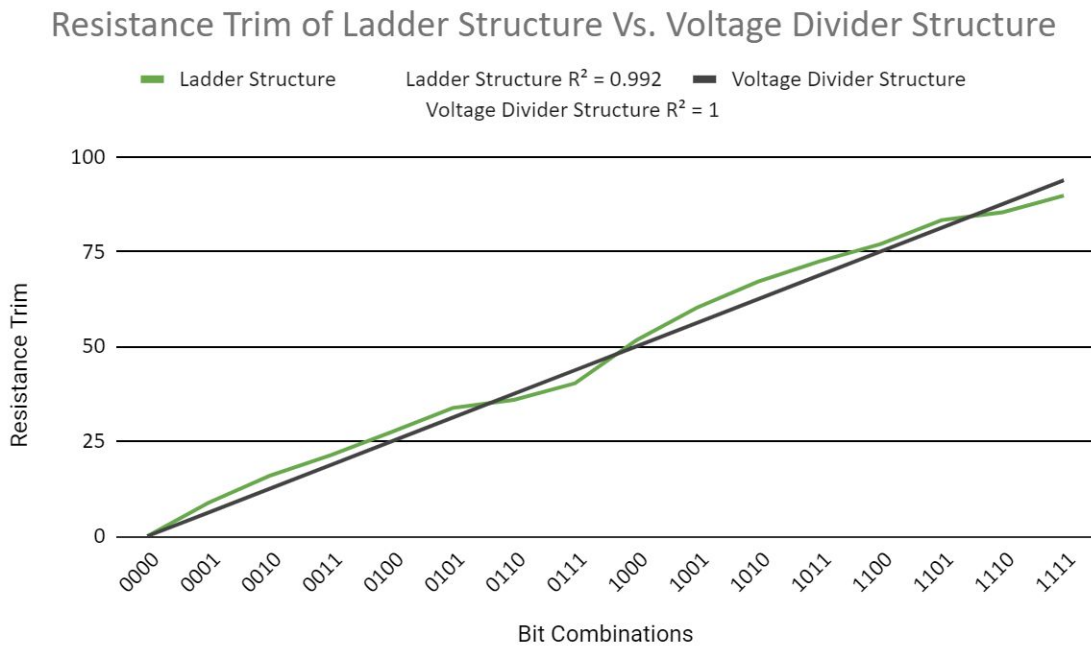


Figure 5.6.2

Both of these structures show that there is a good fit to the ideal values based on the R-squared results. The Ladder Structure is noticeably lacking in the accuracy in many places and the linearity breaks down somewhat. The voltage divider structure is clearly the most desirable structure in terms of the trimming capabilities.

The next comparison made between the two structures was with TCV. The temperature range used for TCV calculation was from 27 to 28 °C. This comparison can be seen in figure 5.6.3 where the x-axis is bit combinations and the y-axis is the TCV in ppm/°C.

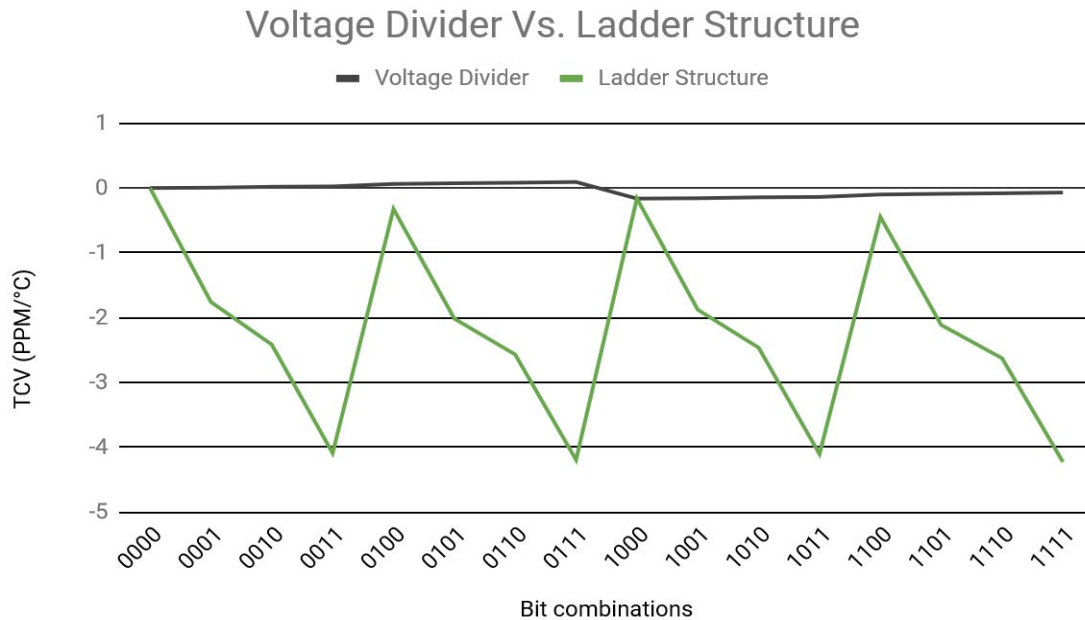


Figure 5.6.3

The closer the TCV is to zero the better performance the circuit has. When looking at the results in figure 5.6.3 we can see that the voltage divider's TCV hovering around 0 ppm/°C for all bit combinations. When looking at the performance of the ladder structure, the TCV jumps around a bit as the bit combination is changed.

The comparison of data results in very interesting conclusions. Of the many structure designs ideated, drafted, tested, and evaluated, the voltage divider structure produces the more desirable result. The specifications of the voltage divider structure include a resolution of a $\pm 1\%$ trim broken down into 4-bits or 16 incremental trimming steps. The R-squared value for this structure is 1 meaning the accuracy and trim quality is basically ideal. The TCV and total resistance area data shows that it performs the best in these evaluation criteria as well. Overall, the voltage divider structure is the High-Resolution Digitally Trimmable Resistor of choice.

6. Closing Material

6.1 CONCLUSION

The High Resolution Trimmable Resistor Project primarily focuses on eight things:

1. Completely understanding the problem that the client needed a solution for and developing an approach/timeline.
2. Defining and obtaining the essentials needed to complete the project
3. Reviewing engineering fundamentals and researching possible solutions to the task that was given to us. This also includes researching current solutions available on the market to see what went right and what went wrong.
4. Ideate some circuits that could meet the requirements of the project and establish thorough testing.
5. Determine the designs which prove promising results and dismiss the undesirable designs.
6. Scale up potential designs and re-test for evaluation.
7. Select final two potential designs and create full scale 4-bit 1% trim designs.
8. Fully test, evaluate, and determine the best design for the project.

The goal of our project is to develop a high-resolution digitally trimmable resistor. The resolution of the resistor should be $\pm 1\%$ and the value of the resistance should be controlled by an 4-bit boolean input. The reason why this is an important project is due to the numerous applications throughout the semiconductor industry where such a device is needed. There are multiple methods for this device but each method has its own drawback. We want to improve upon the temperature coefficient and the resolution of the currently available circuits to create a new trimmable resistor that is still cheap with a new architecture.

We believe that the best plan of action to achieve our goals is the following:

- Meet with our advisor to discuss technical goals, progress, and to make changes as needed.
- Research existing designs and review our fundamentals.
- Ideate and discuss ideas our team brainstormed.
- Simulate reference designs and acquire their temperature coefficients.
- Simulate our designs and compare them to the reference design performance.
- Pick the most promising design based on performance characteristics and hone it into a finished product.
- Prepare final presentation and documentation.

We cannot say that this plan of action surpasses all others (that would be a rather large assertion), but it is a good plan for the following reasons:

- It is efficient because we start small scale and work our way up (as opposed to trying to handle it all at once and failing)

- It is smart because we take the time to look at other designs to see how they could apply to our particular problem. This reduces unnecessary effort on our part.
- It allows us to establish a good timeline.
- It is a complete plan of action.

To conclude, this project applied research in various areas to determine the best approach. The ideation played a critical role in the path of the project in order to create or re-engineer some reference or current industry solutions. The testbench was another important role in this project. The need to evaluate these designs in ways that could completely determine the best result required many different testing aspects that encompassed the strengths and weaknesses of each design. This project took an unbiased approach to comparing the test data and appropriately evaluating each design in order select the final design.

6.2 REFERENCES

- [1] A. Hastings, *The art of analog layout*. Upper Saddle River, NJ: Prentice Hall, 2011.
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- [3] A. S. Sedra and K. C. Smith, *Microelectronic circuits*. New York: Oxford University Press, 2015.
- [4] Cardiac Pacemakers, Inc., 2020. *Digitally Trimmable Resistor For Bandgap Voltage Reference*. US6381491B1.
- [5] J.R. Naylor, ‘R/2r ladder circuit and method for digital-to-analog converter’, WO1999026345A1, 1999.
- [6] O.L. Neel, P. Dumont-Girard, C. Niu, F. Wang, M. Arnoux, ‘Dual thin film precision resistance trimming’ US8242876B2, 2012.
- [7] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI DESIGN TECHNIQUES FOR ANALOG AND DIGITAL CIRCUITS*.
- [8] J. Y. W. Seto, “The electrical properties of polycrystalline silicon films,” *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.

7. Appendices

7.1 APPENDIX 1: OPERATION MANUAL

This operation manual will walk you through the testing of one of the reference circuit designs used in this project. The first step is to open MATLAB and change the Current Folder to the location of the Ladder4bit.m script file. Then, navigate to the Initialize section of the script and enter desired values for the resistors and switch resistance (referencing this schematic and script example shown below).

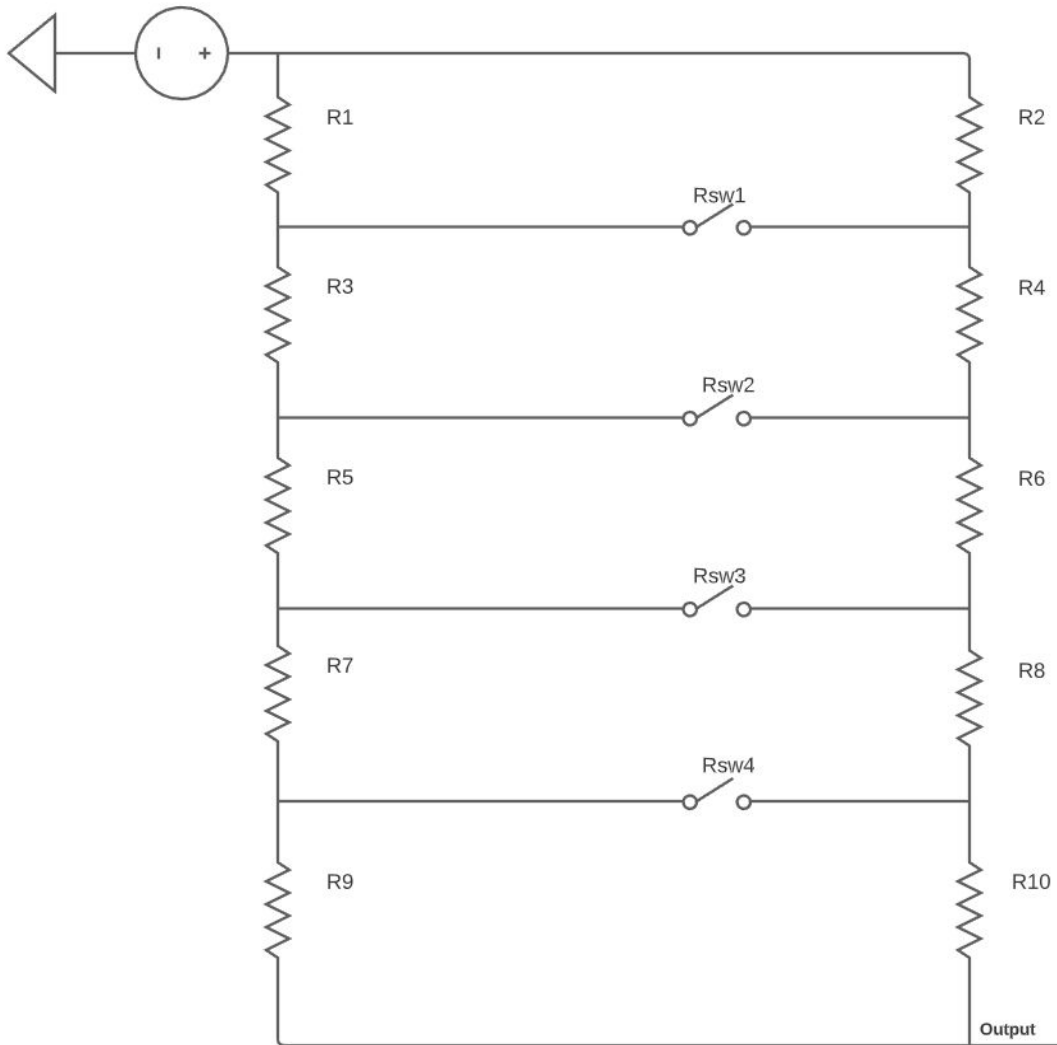


Figure 7.1.1

```

%% Initialize
%-----
%-----

PAR.Vdd = 1; % (volt) Input voltage
PAR.Rtotal = 10000; % (Ohms) Base Value of the trimmable resistor
PAR.Rload = 10000; % (Ohms) Resistor for testing in voltage divider

R1 = 500; % (Ohms) Resistor to Calibrate
R2 = 600; % (Ohms) Resistor to Calibrate
R3 = 4000; % (Ohms) Resistor to Calibrate
R4 = 5000; % (Ohms) Resistor to Calibrate
R5 = 8000; % (Ohms) Resistor to Calibrate
R6 = 1000; % (Ohms) Resistor to Calibrate
R7 = 900; % (Ohms) Resistor to Calibrate
R8 = 1000; % (Ohms) Resistor to Calibrate
R9 = (PAR.Rtotal*2)-R1-R3-R5-R7; % (Ohms) Resistor to Calibrate but done automatically
R10 = (PAR.Rtotal*2)-R2-R4-R6-R8; % (Ohms) Resistor to Calibrate but done automatically
R = [R1,R2,R3,R4,R5,R6,R7,R8,R9,R10]; % (Ohms) Array to input into LadderDyn function

Rsw1 = 2000; % (Ohms) Rung Resistor and/or Switch Resistance
Rsw2 = 2000; % (Ohms) Rung Resistor and/or Switch Resistance
Rsw3 = 2000; % (Ohms) Rung Resistor and/or Switch Resistance
Rsw4 = 2000; % (Ohms) Rung Resistor and/or Switch Resistance
Rsw = [Rsw1,Rsw2,Rsw3,Rsw4]; % (Ohms) Array to input into LadderDyn function

```

Figure 7.1.2 (Initialization section of the MATLAB script)

The script can then be run by pressing the F5 key and the Command Window will print out a matrix detailing the 16 trim configurations in rows with information like actual trim and ideal trim values listed in the subsequent columns. Once this data has been collected and the desired values are achieved, open Cadence Virtuoso and open the 4-Bit ladder structure schematic, and input the desired resistor values.

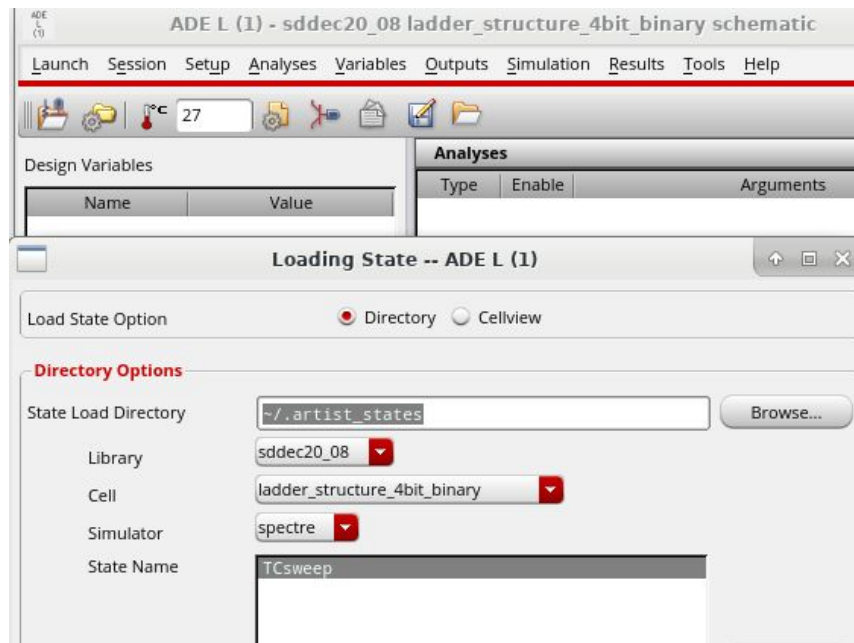


Figure 7.1.3

Opening the TCsweep load state will include the variables required to access the various trimming states of the circuit. Once the ADE L is configured, the parametric analysis can be opened through the tools menu in ADE L. Then load the parametric file within the circuit schematic folder as shown below.

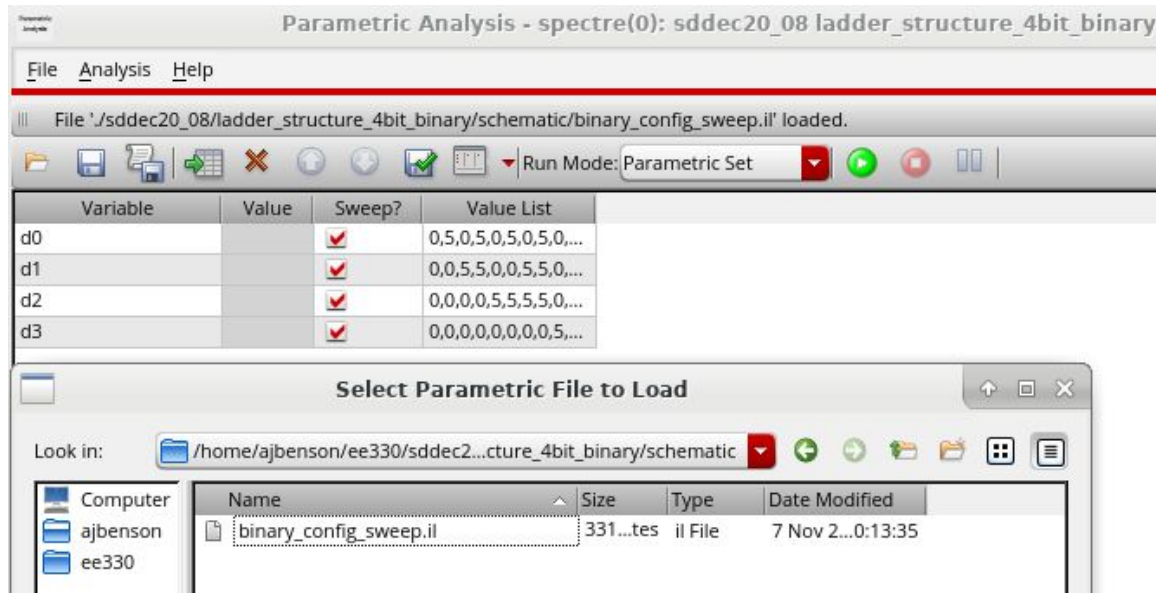


Figure 7.1.4

The environment is now ready to be simulated. Once the binary configurations have been simulated you can export the voltage data to csv to do TCV calculations and analyze the temperature dependencies of the circuit design. This dependency is calculated using the formula for TCV and can be calculated using the excel calculation file as shown below.

Simulate				Calculate		Performance		
State	Temp	V	I	Resistance	Trim	TCR	TCV	% Trim
OFF OFF	27.00	0.49999999990	0.00005000000	10,000.00	0.00	1500.0001	0.0000	0.00%
OFF OFF	28.00	0.49999999989	0.00004992511	10,015.00				

Figure 7.1.5

This calculation is done using the TCV formula:

$$TCV_O = \frac{V_{max} - V_{min}}{V_{nominal}(T_{max} - T_{min})} \times 10^6$$

When analyzing the circuit design to determine its performance make sure to take into consideration the trim quality including its accuracy, monotonicity, and resolution; the temperature dependencies; the total resistance area; and the scalability of the design.

7.2 APPENDIX 2: ALTERNATIVE VERSIONS

The original design considered for making a digitally controllable trimmable resistor was the ladder structure. This structure held high hopes for TCV performance and physical size requirements. But during the project our team was able to make a circuit that outperformed the ladder structure; therefore, the ladder structure was not picked to be the final product of this project. Figure 5.6.2 and 5.6.3 show a comparison of the performance between the two structures and explain why the voltage divider won.

7.3 APPENDIX 3: OTHER CONSIDERATIONS

This senior design project was a research driven project, so the approach taken and the results wanted were constantly changing. Initially, the project seemed to only require knowledge from just EE201, which was later found out to not be totally true. Much more knowledge would be needed, especially in evaluating simulations results.

Scalability of designs is another factor to take into account for these designs. If we chose to design, test, and evaluate extra bits on the structures, the evaluation could change. We understand that increasing resolution on the ladder structure will increase temperature effects of the design. We also know that increasing resolution on the voltage divider will increase the total resistance area of the design. The resistance area factor is not easy to compensate for, but temperature effects can be compensated for by increasing the switch sizes. We don't know the exact effects of these changes, but it appears that increasing resolution and scaling up the designs will be more effective with the ladder structure design.

Related Products:

Virtuoso for circuit designs (Website PDF Link):

<http://home.engineering.iastate.edu/~yulong/EE501lab/Cadence%20analog%20design%20environment%20user%20guide%202006.pdf>

Spectre for circuit analysis (Website PDF Link):

http://eece.cu.edu.eg/~fhussien/Spectre_tutorial.pdf

Related Literature:

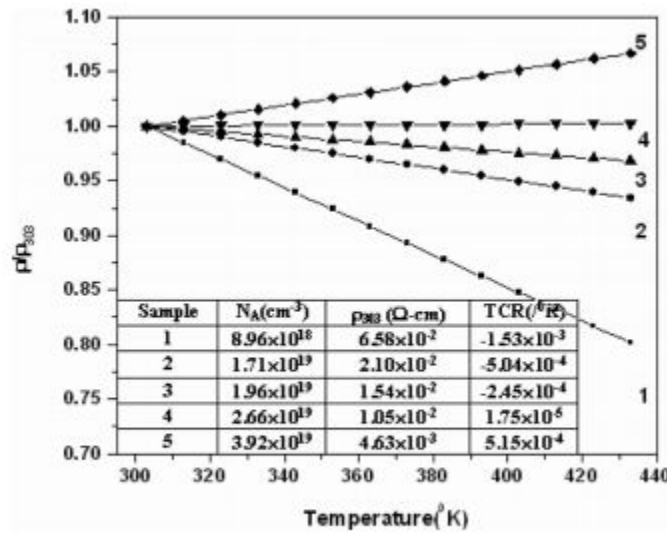


Figure 7.3.1

Normalized resistivity versus temperature for ion-implanted samples

TABLE I. Trapping state density and energy barrier height for three samples with different doping concentrations.

Doping concentration	Energy barrier, E_B	Trapping state density, Q_t
$5 \times 10^{18}/\text{cm}^3$	0.0335 eV	$2.98 \times 10^{12}/\text{cm}^2$
$1 \times 10^{19}/\text{cm}^3$	0.022 eV	$3.41 \times 10^{12}/\text{cm}^2$
$5 \times 10^{19}/\text{cm}^3$	0.005 eV	$3.64 \times 10^{12}/\text{cm}^2$

Figure 7.3.2

Energy barrier and State density for Doping concentrations

Eq. (13) the conductivity of a polysilicon film with a grain size L cm is

$$\sigma = Lq^2p_a \left(\frac{1}{2\pi m^* kT} \right)^{1/2} \exp\left(-\frac{qV_B}{kT}\right). \quad (14)$$

Inserting Eqs. (6) and (11) into Eq. (14), we find that

$$\sigma \propto \exp[-(\frac{1}{2}E_t - E_f)/kT], \quad \text{if } NL < Q_t, \quad (15)$$

$$\sigma \propto T^{-1/2} \exp(-E_B/kT), \quad \text{if } NL > Q_t. \quad (16)$$

Figure 7.3.3

Polysilicon conductivity equations

7.4 APPENDIX 4: CODE (READ PAGE BY PAGE)

```

%% Iowa State University
% Author : Pierce Nablo, Alek Benson
% e-mail : pnbloo7@iastate.edu, ajbenson@iastate.edu
%
% Project Sponsor : Iowa State University
%
% Award/Contract Number : Digitally Trimmable Resistor
% Binary trim going to a 1% trim total
%
% Period of Performance : Until MATLAB pushes out update
and breaks code
%
% Department: Electrical and Computer Engineering (ECpE)
%
%% Description:
%-----
% Simulation of a 4-bit ladder structure in order to calculate the
resistance
% value of R2,R4,R6,R8,R10 in the ladder structure to achieve a
1% percent trim
%
% First:
% Set switch resistance for sw1,sw2,sw3,sw4
% Second:
% Manually manipulate R2, R4, R6, R8 until trim is as desired
%
%% Prepare system
%-----
%-----
close all;
clear all;

%% Initialize
%-----
%-----

PAR.Vdd = 1; % (volt) Input voltage
PAR.Rtotal = 10000; % (Ohms) Base Value of the trimmable
resistor
PAR.Rload = 10000; % (Ohms) Resistor for testing in voltage
divider

R1 = 150; % (Ohms) Resistor to Calibrate
R2 = 342.8; % (Ohms) Resistor to Calibrate

R3 = 1200; % (Ohms) Resistor to Calibrate
R4 = 1448.6; % (Ohms) Resistor to Calibrate

R5 = 14000; % (Ohms) Resistor to Calibrate
R6 = 14434;

R9 = 500; % (Ohms) Resistor to
Calibrate but done automatically
R10 = 10; % (Ohms) Resistor to Calibrate

R7 = (PAR.Rtotal*2)-R1-R3-R5-R9; %
(Ohms) Resistor to Calibrate
R8 = (PAR.Rtotal*2)-R2-R4-R6-R10; % (Ohms)
Resistor to Calibrate
R = [R1,R2,R3,R4,R5,R6,R7,R8,R9,R10]; % (Ohms) Array to
input into LadderDyn function

Rsw1 = 900; % (Ohms) Rung Resistor and/or Switch
Resistance
Rsw2 = 800; % (Ohms) Rung Resistor and/or
Switch Resistance
Rsw3 = 700; % (Ohms) Rung Resistor and/or Switch
Resistance
Rsw4 = 600; % (Ohms) Rung Resistor and/or
Switch Resistance
Rsw = [Rsw1,Rsw2,Rsw3,Rsw4]; % (Ohms) Array to input into
LadderDyn function

%% Run
%-----
%-----

% Calculate Vout, Iout given difference bit combinations
LadderData = LadderDyn(R,Rsw,PAR);

% Calculate Trim given Resistance of ladder structure
TrimPerf = LadderPerformance(LadderData,PAR);

%Display TrimPerf as double
sprintf('____Bit____Trim____Ideal____Trim
perc____Trim_chg_')
format shortG
double(TrimPerf)

x = 0:1:15;
plot(x,TrimPerf(:,2))
hold on
plot(x,TrimPerf(:,3))
hold off
xlabel('Bit Combination');
ylabel('Ohms Trim');

%% Ladder Function
%-----
%-----
function [Y] = LadderDyn(R,Rsw,PAR)
%% SW1=OFF;SW2=OFF;SW3=OFF;SW4=OFF;
Vout_0000 ; Iout_0000
%-----
%-----
Rx_0000 = R(1) + R(3) + R(5) + R(7) + R(9); % Left leg
Ry_0000 = R(2) + R(4) + R(6) + R(8) + R(10); % Right leg

% Left & Right leg in parallel
Req_0000 = (1/Rx_0000 + 1/Ry_0000)^(-1);

% Outputs for Y
VVout_0000 = (PAR.Vdd*PAR.Rload)/(PAR.Rload+Req_0000);
IIout_0000 = PAR.Vdd/(PAR.Rload+Req_0000);
Req_0000 = (PAR.Vdd - VVout_0000)/IIout_0000;
%-----
%-----
%% SW1=ON;SW2=OFF;SW3=OFF;SW4=OFF;
Vout_0001 ; Iout_0001
%-----
%-----
% Combine series resistors where able
Rx_0001 = R(3) + R(5) + R(7) + R(9); % Left leg
Ry_0001 = R(4) + R(6) + R(8) + R(10); % Right leg

```



```

% Node A
% Ir1 == Isw1 + Irx;
% Node B
% Ir2 + Isw1 == Iry;
% Node Vout
% Irx + Iry == Irl;

% System of equations
syms Va_0001 Vb_0001 Vout_0001
eqn1_0001 = (PAR.Vdd-Va_0001)/(R(1)) ==
(Va_0001-Vb_0001)/(Rsw(1)) +
(Va_0001-Vout_0001)/(Rx_0001);
eqn2_0001 = (PAR.Vdd-Vb_0001)/(R(2)) +
(Va_0001-Vb_0001)/(Rsw(1)) ==
(Vb_0001-Vout_0001)/(Ry_0001);
eqn3_0001 = (Va_0001-Vout_0001)/(Rx_0001) +
(Vb_0001-Vout_0001)/(Ry_0001) == (Vout_0001)/(PAR.Rload);

% Solve system of equations
sol_0001 = solve([eqn1_0001,eqn2_0001,eqn3_0001],
[Va_0001,Vb_0001,Vout_0001]);

% Outputs for Y
VVout_0001 = sol_0001.Vout_0001;
IIout_0001 = VVout_0001/PAR.Rload;
Req_0001 = (PAR.Vdd - VVout_0001)/IIout_0001;
%-----
%-----
%% SW1=OFF;SW2=ON;SW3=OFF;SW4=OFF;
Vout_0010 ; Iout_0010
%-----
%-----
% Combine series resistors where able
Rx_0010 = R(1) + R(3); % Left leg
Ry_0010 = R(2) + R(4); % Right leg
Rxx_0010 = R(5) + R(7) + R(9); % Left leg Lower
Ryy_0010 = R(6) + R(8) + R(10); % Right leg Lower

% Node C
% Irx == Isw2 + Irx;
% Node D
% Iry + Isw2 == Iry;
% Node Vout
% Irx + Iry == Irl;

% System of equations
syms Vc_0010 Vd_0010 Vout_0010
eqn1_0010 = (PAR.Vdd-Vc_0010)/(Rx_0010) ==
(Vc_0010-Vd_0010)/(Rsw(2)) +
(Vc_0010-Vout_0010)/(Rxx_0010);
eqn2_0010 = (PAR.Vdd-Vd_0010)/(Ry_0010) +
(Vc_0010-Vd_0010)/(Rsw(2)) ==
(Vd_0010-Vout_0010)/(Ryy_0010);
eqn3_0010 = (Vc_0010-Vout_0010)/(Rxx_0010) +
(Vd_0010-Vout_0010)/(Ryy_0010) == (Vout_0010)/(PAR.Rload);

% Solve system of equations
sol_0010 = solve([eqn1_0010,eqn2_0010,eqn3_0010],
[Vc_0010,Vd_0010,Vout_0010]);

% Outputs for Y
VVout_0010 = sol_0010.Vout_0010;
IIout_0010 = VVout_0010/PAR.Rload;
Req_0010 = (PAR.Vdd - VVout_0010)/IIout_0010;
%-----
%-----

```

```

%% SW1=ON;SW2=ON;SW3=OFF;SW4=OFF; Vout_001
; Iout_001
%-----
%-----
% Combine series resistors where able
Rx_0010 = R(5) + R(7) + R(9); % Left leg
Ry_0010 = R(6) + R(8) + R(10); % Right leg

% Node A
% Ir1 == Isw1 + Ir3;
% Node B
% Ir2 + Isw1 == Ir4;
% Node C
% Ir3 == Isw2 + Ir5;
% Node D
% Ir4 + Isw2 == Ir6;
% Node Vout
% Ir5 + Ir6 == Irl;

% System of equations
syms Va_0010 Vb_0010 Vc_0010 Vd_0010 Vout_0010
eqn1_0010 = (PAR.Vdd-Va_0010)/(R(1)) ==
(Va_0010-Vb_0010)/(Rsw(1)) + (Va_0010-Vc_0010)/(R(3));
eqn2_0010 = (PAR.Vdd-Vb_0010)/(R(2)) +
(Va_0010-Vb_0010)/(Rsw(1)) == (Vb_0010-Vd_0010)/(R(4));
eqn3_0010 = (Va_0010-Vc_0010)/(R(3)) ==
(Vc_0010-Vd_0010)/(Rsw(2)) +
(Vc_0010-Vout_0010)/(Rx_0010);
eqn4_0010 = (Vb_0010-Vd_0010)/(R(4)) +
(Vc_0010-Vd_0010)/(Rsw(2)) ==
(Vd_0010-Vout_0010)/(Ry_0010);
eqn5_0010 = (Vc_0010-Vout_0010)/(Rx_0010) +
(Vd_0010-Vout_0010)/(Ry_0010) == (Vout_0010)/(PAR.Rload);

% Solve system of equations
sol_0010 =
solve([eqn1_0010,eqn2_0010,eqn3_0010,eqn4_0010,eqn5_0010],
[Va_0010,Vb_0010,Vc_0010,Vd_0010,Vout_0010]);

% Outputs for Y
VVout_0010 = sol_0010.Vout_0010;
IIout_0010 = VVout_0010/PAR.Rload;
Req_0010 = (PAR.Vdd - VVout_0010)/IIout_0010;
%-----
%-----
%% SW1=OFF;SW2=OFF;SW3=ON;SW4=OFF;
Vout_0100 ; Iout_0100
%-----
%-----
% Combine series resistors where able
Rx_0100 = R(1) + R(3) + R(5); % Left leg
Ry_0100 = R(2) + R(4) + R(6); % Right leg
Rxx_0100 = R(7) + R(9); % Left leg Lower
Ryy_0100 = R(8) + R(10); % Right leg Lower

% Node E
% Irx == Isw3 + Irx;
% Node F
% Iry + Isw3 == Iry;
% Node Vout
% Irx + Iry == Irl;

% System of equations
syms Ve_0100 Vf_0100 Vout_0100
eqn1_0100 = (PAR.Vdd-Ve_0100)/(Rx_0100) ==
(Ve_0100-Vf_0100)/(Rsw(3)) +
(Ve_0100-Vout_0100)/(Rxx_0100);

```

```

    eqn2_0100 = (PAR.Vdd-Vf_0100)/(Ry_0100) +
(Ve_0100-Vf_0100)/(Rsw(3)) ==
(Vf_0100-Vout_0100)/(Ryy_0100);
    eqn3_0100 = (Ve_0100-Vout_0100)/(Rxx_0100) +
(Vf_0100-Vout_0100)/(Ryy_0100) == (Vout_0100)/(PAR.Rload);

    % Solve system of equations
    sol_0100 = solve([eqn1_0100,eqn2_0100,eqn3_0100],
[Ve_0100,Vf_0100,Vout_0100]);

    % Outputs for Y
    VVout_0100 = sol_0100.Vout_0100;
    Iout_0100 = VVout_0100/PAR.Rload;
    Req_0100 = (PAR.Vdd - VVout_0100)/Iout_0100;
    %-----
    %-----
    %% SW1=ON;SW2=OFF;SW3=ON;SW4=OFF;    Vout_0101
; Iout_0101
    %-----
    %-----
    % Combine series resistors where able
    Rx_0101 = R(3) + R(5);    % Left leg
    Ry_0101 = R(4) + R(6);    % Right leg
    Rxx_0101 = R(7) + R(9);    % Left leg
    Ryy_0101 = R(8) + R(10);    % Right leg

    % Node A
    % Ir1 == Isw1 + Irx;
    % Node B
    % Ir2 + Isw1 == Iry;
    % Node E
    % Irx == Isw3 + Irxx;
    % Node F
    % Iry + Isw3 == Iryy;
    % Node Vout
    % Irxx + Iryy == Irl;

    % System of equations
    syms Va_0101 Vb_0101 Ve_0101 Vf_0101 Vout_0101
    eqn1_0101 = (PAR.Vdd-Va_0101)/(R(1)) ==
(Va_0101-Vb_0101)/(Rsw(1)) + (Va_0101-Ve_0101)/(Rx_0101);
    eqn2_0101 = (PAR.Vdd-Vb_0101)/(R(2)) +
(Va_0101-Vb_0101)/(Rsw(1)) == (Vb_0101-Vf_0101)/(Ry_0101);
    eqn3_0101 = (Va_0101-Ve_0101)/(Rx_0101) ==
(Ve_0101-Vf_0101)/(Rsw(3)) + (Ve_0101-Vout_0101)/(Rxx_0101);
    eqn4_0101 = (Vb_0101-Vf_0101)/(Ry_0101) +
(Ve_0101-Vf_0101)/(Rsw(3)) == (Vf_0101-Vout_0101)/(Ryy_0101);
    eqn5_0101 = (Ve_0101-Vout_0101)/(Rxx_0101) +
(Vf_0101-Vout_0101)/(Ryy_0101) == (Vout_0101)/(PAR.Rload);

    % Solve system of equations
    sol_0101 =
solve([eqn1_0101,eqn2_0101,eqn3_0101,eqn4_0101,eqn5_0101],
[Va_0101,Vb_0101,Ve_0101,Vf_0101,Vout_0101]);

    % Outputs for Y
    VVout_0101 = sol_0101.Vout_0101;
    Iout_0101 = VVout_0101/PAR.Rload;
    Req_0101 = (PAR.Vdd - VVout_0101)/Iout_0101;
    %-----
    %-----
    %% SW1=OFF;SW2=ON;SW3=ON;SW4=OFF;    Vout_0100
; Iout_0100
    %-----
    %-----
    % Combine series resistors where able
    Rx_0100 = R(1) + R(3);    % Left leg

```

```

Ry_0100 = R(2) + R(4);    % Right leg
Rxx_0100 = R(7) + R(9);    % Left leg
Ryy_0100 = R(8) + R(10);    % Right leg

    % Node C
    % Irx == Isw2 + Ir5;
    % Node D
    % Iry + Isw2 == Ir6;
    % Node E
    % Ir5 == Isw3 + Irxx;
    % Node F
    % Ir6 + Isw3 == Iryy;
    % Node Vout
    % Irxx + Iryy == Irl;

    % System of equations
    syms Vc_0100 Vd_0100 Ve_0100 Vf_0100 Vout_0100
    eqn1_0100 = (PAR.Vdd-Vc_0100)/(Rx_0100) ==
(Vc_0100-Vd_0100)/(Rsw(2)) + (Vc_0100-Ve_0100)/(R(5));
    eqn2_0100 = (PAR.Vdd-Vd_0100)/(Ry_0100) +
(Vc_0100-Vd_0100)/(Rsw(2)) == (Vd_0100-Vf_0100)/(R(6));
    eqn3_0100 = (Vc_0100-Ve_0100)/(R(5)) ==
(Ve_0100-Vf_0100)/(Rsw(3)) + (Ve_0100-Vout_0100)/(Rxx_0100);
    eqn4_0100 = (Vd_0100-Vf_0100)/(R(6)) +
(Ve_0100-Vf_0100)/(Rsw(3)) == (Vf_0100-Vout_0100)/(Ryy_0100);
    eqn5_0100 = (Ve_0100-Vout_0100)/(Rxx_0100) +
(Vf_0100-Vout_0100)/(Ryy_0100) == (Vout_0100)/(PAR.Rload);

    % Solve system of equations
    sol_0100 =
solve([eqn1_0100,eqn2_0100,eqn3_0100,eqn4_0100,eqn5_0100],
[Vc_0100,Vd_0100,Ve_0100,Vf_0100,Vout_0100]);

    % Outputs for Y
    VVout_0100 = sol_0100.Vout_0100;
    Iout_0100 = VVout_0100/PAR.Rload;
    Req_0100 = (PAR.Vdd - VVout_0100)/Iout_0100;
    %-----
    %-----
    %% SW1=ON;SW2=ON;SW3=ON;SW4=OFF;    Vout_0101
; Iout_0101
    %-----
    %-----
    % Combine series resistors where able
    Rx_0101 = R(7) + R(9);    % Left leg
    Ry_0101 = R(8) + R(10);    % Right leg

    % Node A
    % Ir1 == Isw1 + Ir3;
    % Node B
    % Ir2 + Isw1 == Ir4;
    % Node C
    % Ir3 == Isw2 + Ir5;
    % Node D
    % Ir4 + Isw2 == Ir6;
    % Node E
    % Ir5 == Isw3 + Irx;
    % Node F
    % Ir6 + Isw3 == Iry;
    % Node Vout
    % Irx + Iry == Irl;

    % System of equations
    syms Va_0101 Vb_0101 Vc_0101 Vd_0101 Ve_0101 Vf_0101 Vout_0101
    eqn1_0101 = (PAR.Vdd-Va_0101)/(R(1)) ==
(Va_0101-Vb_0101)/(Rsw(1)) + (Va_0101-Vc_0101)/(R(3));

```

```

eqn2_011 = (PAR.Vdd-Vb_011)/(R(2)) +
(Va_011-Vb_011)/(Rsw(1)) == (Vb_011-Vd_011)/(R(4));
eqn3_011 = (Va_011-Vc_011)/(R(3)) ==
(Vc_011-Vd_011)/(Rsw(2)) + (Vc_011-Ve_011)/(R(5));
eqn4_011 = (Vb_011-Vd_011)/(R(4)) +
(Vc_011-Vd_011)/(Rsw(2)) == (Vd_011-Vf_011)/(R(6));
eqn5_011 = (Vc_011-Ve_011)/(R(5)) ==
(Ve_011-Vf_011)/(Rsw(3)) + (Ve_011-Vout_011)/(Rx_011);
eqn6_011 = (Vd_011-Vf_011)/(R(6)) +
(Ve_011-Vf_011)/(Rsw(3)) == (Vf_011-Vout_011)/(Ry_011);
eqn7_011 = (Ve_011-Vout_011)/(Rx_011) +
(Vf_011-Vout_011)/(Ry_011) == (Vout_011)/(PAR.Rload);

```

```

% Solve system of equations
sol_011 =
solve([eqn1_011,eqn2_011,eqn3_011,eqn4_011,eqn5_011,eqn6_011,
eqn7_011],
[Va_011,Vb_011,Vc_011,Vd_011,Ve_011,Vf_011,Vout_011]);

```

```

% Outputs for Y
VVout_011 = sol_011.Vout_011;
Iout_011 = VVout_011/PAR.Rload;
Req_011 = (PAR.Vdd - VVout_011)/Iout_011;
%-----
%-----
%% SW1=OFF;SW2=OFF;SW3=OFF;SW4=ON;

```

```

Vout_1000 ; Iout_1000
%-----
%-----
% Combine series resistors where able
Rx_1000 = R(1)+ R(3) + R(5) + R(7); % Left leg
Ry_1000 = R(2)+ R(4) + R(6) + R(8); % Right leg

```

```

% Node G
% Irx == Isw4 + Ir9;
% Node H
% Iry + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

```

```

% System of equations
syms Vg_1000 Vh_1000 Vout_1000
eqn1_1000 = (PAR.Vdd-Vg_1000)/(Rx_1000) ==
(Vg_1000-Vh_1000)/(Rsw(4)) + (Vg_1000-Vout_1000)/(R(9));
eqn2_1000 = (PAR.Vdd-Vh_1000)/(Ry_1000) +
(Vg_1000-Vh_1000)/(Rsw(4)) == (Vh_1000-Vout_1000)/(R(10));
eqn3_1000 = (Vg_1000-Vout_1000)/(R(9)) +
(Vh_1000-Vout_1000)/(R(10)) == (Vout_1000)/(PAR.Rload);

```

```

% Solve system of equations
sol_1000 = solve([eqn1_1000,eqn2_1000,eqn3_1000],
[Vg_1000,Vh_1000,Vout_1000]);

```

```

% Outputs for Y
VVout_1000 = sol_1000.Vout_1000;
Iout_1000 = VVout_1000/PAR.Rload;
Req_1000 = (PAR.Vdd - VVout_1000)/Iout_1000;
%-----
%-----
%% SW1=ON;SW2=OFF;SW3=OFF;SW4=ON; Vout_1001
; Iout_1001

```

```

%-----
%-----
% Combine series resistors where able
Rx_1001 = R(3) + R(5) + R(7); % Left leg
Ry_1001 = R(4) + R(6) + R(8); % Right leg

```

```

% Node A
% Ir1 == Isw1 + Irx;
% Node B
% Ir2 + Isw1 == Iry;
% Node G
% Irx == Isw4 + Ir9;
% Node H
% Iry + Isw4 == Ir10;
% Node Vout
% Irx9 + Ir10 == Irl;

```

```

% System of equations
syms Va_1001 Vb_1001 Vg_1001 Vh_1001 Vout_1001
eqn1_1001 = (PAR.Vdd-Va_1001)/(R(1)) ==
(Va_1001-Vb_1001)/(Rsw(1)) + (Va_1001-Vg_1001)/(Rx_1001);
eqn2_1001 = (PAR.Vdd-Vb_1001)/(R(2)) +
(Va_1001-Vb_1001)/(Rsw(1)) == (Vb_1001-Vh_1001)/(Ry_1001);
eqn3_1001 = (Va_1001-Vg_1001)/(Rx_1001) ==
(Vg_1001-Vh_1001)/(Rsw(4)) + (Vg_1001-Vout_1001)/(R(9));
eqn4_1001 = (Vb_1001-Vh_1001)/(Ry_1001) +
(Vg_1001-Vh_1001)/(Rsw(4)) == (Vh_1001-Vout_1001)/(R(10));
eqn5_1001 = (Vg_1001-Vout_1001)/(R(9)) +
(Vh_1001-Vout_1001)/(R(10)) == (Vout_1001)/(PAR.Rload);

```

```

% Solve system of equations
sol_1001 =
solve([eqn1_1001,eqn2_1001,eqn3_1001,eqn4_1001,eqn5_1001],
[Va_1001,Vb_1001,Vg_1001,Vh_1001,Vout_1001]);

```

```

% Outputs for Y
VVout_1001 = sol_1001.Vout_1001;
Iout_1001 = VVout_1001/PAR.Rload;
Req_1001 = (PAR.Vdd - VVout_1001)/Iout_1001;
%-----
%-----
%% SW1=OFF;SW2=ON;SW3=OFF;SW4=ON; Vout_1010
; Iout_1010

```

```

%-----
%-----
% Combine series resistors where able
Rx_1010 = R(1) + R(3); % Left leg
Ry_1010 = R(2) + R(4); % Right leg
Rxx_1010 = R(5) + R(7); % Left leg
Ryy_1010 = R(6) + R(8); % Right leg

```

```

% Node C
% Ir1 == Isw2 + Irx;
% Node D
% Ir2 + Isw2 == Iry;
% Node G
% Irx == Isw4 + Irxx;
% Node H
% Iry + Isw4 == Iryy;
% Node Vout
% Irxx + Iryy == Irl;

```

```

% System of equations
syms Vc_1010 Vd_1010 Vg_1010 Vh_1010 Vout_1010
eqn1_1010 = (PAR.Vdd-Vc_1010)/(Rx_1010) ==
(Vc_1010-Vd_1010)/(Rsw(2)) + (Vc_1010-Vg_1010)/(Rxx_1010);
eqn2_1010 = (PAR.Vdd-Vd_1010)/(Ry_1010) +
(Vc_1010-Vd_1010)/(Rsw(2)) == (Vd_1010-Vh_1010)/(Ryy_1010);
eqn3_1010 = (Vc_1010-Vg_1010)/(Rxx_1010) ==
(Vg_1010-Vh_1010)/(Rsw(4)) + (Vg_1010-Vout_1010)/(R(9));
eqn4_1010 = (Vd_1010-Vh_1010)/(Ryy_1010) +
(Vg_1010-Vh_1010)/(Rsw(4)) == (Vh_1010-Vout_1010)/(R(10));

```

```

    eqn5_1010 = (Vg_1010-Vout_1010)/(R(9)) +
(Vh_1010-Vout_1010)/(R(10)) == (Vout_1010)/(PAR.Rload);

% Solve system of equations
sol_1010 =
solve([eqn1_1010,eqn2_1010,eqn3_1010,eqn4_1010,eqn5_1010],
[Vc_1010,Vd_1010,Vg_1010,Vh_1010,Vout_1010]);

% Outputs for Y
VVout_1010 = sol_1010.Vout_1010;
Iout_1010 = VVout_1010/PAR.Rload;
Req_1010 = (PAR.Vdd - VVout_1010)/Iout_1010;
%-----
%-----
%% SW1=ON;SW2=ON;SW3=OFF;SW4=ON;    Vout_1011;
Iout_1011
%-----
%-----
% Combine series resistors where able
Rx_1011 = R(5) + R(7);    % Left leg
Ry_1011 = R(6) + R(8);    % Right leg

% Node A
% Ir1 == Isw1 + Ir3;
% Node B
% Ir2 + Isw1 == Ir4;
% Node C
% Ir3 == Isw2 + Irx;
% Node D
% Ir4 + Isw2 == Iry;
% Node G
% Irx == Isw4 + Ir9;
% Node H
% Iry + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

% System of equations
syms Va_1011 Vb_1011 Vc_1011 Vd_1011 Vg_1011 Vh_1011 Vout_1011
eqn1_1011 = (PAR.Vdd-Va_1011)/(R(1)) ==
(Va_1011-Vb_1011)/(Rsw(1)) + (Va_1011-Vc_1011)/(R(3));
eqn2_1011 = (PAR.Vdd-Vb_1011)/(R(2)) +
(Va_1011-Vb_1011)/(Rsw(1)) == (Vb_1011-Vd_1011)/(R(4));
eqn3_1011 = (Va_1011-Vc_1011)/(R(3)) ==
(Vc_1011-Vd_1011)/(Rsw(2)) + (Vc_1011-Vg_1011)/(Rx_1011);
eqn4_1011 = (Vb_1011-Vd_1011)/(R(4)) +
(Vc_1011-Vd_1011)/(Rsw(2)) == (Vd_1011-Vh_1011)/(Ry_1011);
eqn5_1011 = (Vc_1011-Vg_1011)/(Rx_1011) ==
(Vg_1011-Vh_1011)/(Rsw(4)) + (Vg_1011-Vout_1011)/(R(9));
eqn6_1011 = (Vd_1011-Vh_1011)/(Ry_1011) +
(Vg_1011-Vh_1011)/(Rsw(4)) == (Vh_1011-Vout_1011)/(R(10));
eqn7_1011 = (Vg_1011-Vout_1011)/(R(9)) +
(Vh_1011-Vout_1011)/(R(10)) == (Vout_1011)/(PAR.Rload);

% Solve system of equations
sol_1011 =
solve([eqn1_1011,eqn2_1011,eqn3_1011,eqn4_1011,eqn5_1011,eqn6_1011,eqn7_1011],
[Va_1011,Vb_1011,Vc_1011,Vd_1011,Vg_1011,Vh_1011,Vout_1011]);

% Outputs for Y
VVout_1011 = sol_1011.Vout_1011;
Iout_1011 = VVout_1011/PAR.Rload;
Req_1011 = (PAR.Vdd - VVout_1011)/Iout_1011;
%-----
%-----

```

```

%% SW1=OFF;SW2=OFF;SW3=ON;SW4=ON;    Vout_1100
; Iout_1100
%-----
%-----
% Combine series resistors where able
Rx_1100 = R(1) + R(3) + R(5);    % Left leg
Ry_1100 = R(2) + R(4) + R(6);    % Right leg

% Node E
% Irx == Isw3 + Ir7;
% Node F
% Iry + Isw3 == Ir8;
% Node G
% Ir7 == Isw4 + Ir9;
% Node H
% Ir8 + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

% System of equations
syms Ve_1100 Vf_1100 Vg_1100 Vh_1100 Vout_1100
eqn1_1100 = (PAR.Vdd-Ve_1100)/(Rx_1100) ==
(Ve_1100-Vf_1100)/(Rsw(3)) + (Ve_1100-Vg_1100)/(R(7));
eqn2_1100 = (PAR.Vdd-Vf_1100)/(Ry_1100) +
(Ve_1100-Vf_1100)/(Rsw(3)) == (Vf_1100-Vh_1100)/(R(8));
eqn3_1100 = (Ve_1100-Vg_1100)/(R(7)) ==
(Vg_1100-Vh_1100)/(Rsw(4)) + (Vg_1100-Vout_1100)/(R(9));
eqn4_1100 = (Vf_1100-Vh_1100)/(R(8)) +
(Vg_1100-Vh_1100)/(Rsw(4)) == (Vh_1100-Vout_1100)/(R(10));
eqn5_1100 = (Vg_1100-Vout_1100)/(R(9)) +
(Vh_1100-Vout_1100)/(R(10)) == (Vout_1100)/(PAR.Rload);

% Solve system of equations
sol_1100 =
solve([eqn1_1100,eqn2_1100,eqn3_1100,eqn4_1100,eqn5_1100],
[Ve_1100,Vf_1100,Vg_1100,Vh_1100,Vout_1100]);

% Outputs for Y
VVout_1100 = sol_1100.Vout_1100;
Iout_1100 = VVout_1100/PAR.Rload;
Req_1100 = (PAR.Vdd - VVout_1100)/Iout_1100;
%-----
%-----
%% SW1=OFF;SW2=OFF;SW3=ON;SW4=OFF;    Vout_1101
; Iout_1101
%-----
%-----
% Combine series resistors where able
Rx_1101 = R(3) + R(5);    % Left leg
Ry_1101 = R(4) + R(6);    % Right leg

% Node A
% Ir1 == Isw1 + Ir3;
% Node B
% Ir2 + Isw1 == Ir4;
% Node E
% Irx == Isw3 + Ir7;
% Node F
% Iry + Isw3 == Ir8;
% Node G
% Ir7 == Isw4 + Ir9;
% Node H
% Ir8 + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

% System of equations

```

```

syms Va_1101 Vb_1101 Ve_1101 Vf_1101 Vg_1101 Vh_1101 Vout_1101
eqn1_1101 = (PAR.Vdd-Va_1101)/(R(1)) ==
(Va_1101-Vb_1101)/(Rsw(1)) + (Va_1101-Ve_1101)/(Rx_1101);
eqn2_1101 = (PAR.Vdd-Vb_1101)/(R(2)) +
(Va_1101-Vb_1101)/(Rsw(1)) == (Vb_1101-Vf_1101)/(Ry_1101);
eqn3_1101 = (Va_1101-Ve_1101)/(Rx_1101) ==
(Ve_1101-Vf_1101)/(Rsw(3)) + (Ve_1101-Vg_1101)/(R(7));
eqn4_1101 = (Vb_1101-Vf_1101)/(Ry_1101) +
(Ve_1101-Vf_1101)/(Rsw(3)) == (Vf_1101-Vh_1101)/(R(8));
eqn5_1101 = (Ve_1101-Vg_1101)/(R(7)) ==
(Vg_1101-Vh_1101)/(Rsw(4)) + (Vg_1101-Vout_1101)/(R(9));
eqn6_1101 = (Vf_1101-Vh_1101)/(R(8)) +
(Vg_1101-Vh_1101)/(Rsw(4)) == (Vh_1101-Vout_1101)/(R(10));
eqn7_1101 = (Vg_1101-Vout_1101)/(R(9)) +
(Vh_1101-Vout_1101)/(R(10)) == (Vout_1101)/(PAR.Rload);

% Solve system of equations
sol_1101 =
solve([eqn1_1101,eqn2_1101,eqn3_1101,eqn4_1101,eqn5_1101,eqn6_1101,
1,eqn7_1101],
[Va_1101,Vb_1101,Ve_1101,Vf_1101,Vg_1101,Vh_1101,Vout_1101]);

% Outputs for Y
VVout_1101 = sol_1101.Vout_1101;
Iout_1101 = VVout_1101/PAR.Rload;
Req_1101 = (PAR.Vdd - VVout_1101)/Iout_1101;
%-----
%% SW1=OFF;SW2=OFF;SW3=ON;SW4=OFF;    Vout_1101
; Iout_1101
%-----
%-----

% Combine series resistors where able
Rx_1101 = R(1) + R(3);    % Left leg
Ry_1101 = R(2) + R(4);    % Right leg

% Node C
% Irx == Isw2 + Ir5;
% Node D
% Iry + Isw2 == Ir6;
% Node E
% Ir5 == Isw3 + Ir7;
% Node F
% Ir6 + Isw3 == Ir8;
% Node G
% Ir7 == Isw4 + Ir9;
% Node H
% Ir8 + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

% System of equations
syms Vc_1101 Vd_1101 Ve_1101 Vf_1101 Vg_1101 Vh_1101 Vout_1101
eqn1_1101 = (PAR.Vdd-Vc_1101)/(Rx_1101) ==
(Vc_1101-Vd_1101)/(Rsw(2)) + (Vc_1101-Ve_1101)/(R(5));
eqn2_1101 = (PAR.Vdd-Vd_1101)/(Ry_1101) +
(Vc_1101-Vd_1101)/(Rsw(2)) == (Vd_1101-Vf_1101)/(R(6));
eqn3_1101 = (Vc_1101-Ve_1101)/(R(5)) ==
(Ve_1101-Vf_1101)/(Rsw(3)) + (Ve_1101-Vg_1101)/(R(7));
eqn4_1101 = (Vd_1101-Vf_1101)/(R(6)) +
(Ve_1101-Vf_1101)/(Rsw(3)) == (Vf_1101-Vh_1101)/(R(8));
eqn5_1101 = (Ve_1101-Vg_1101)/(R(7)) ==
(Vg_1101-Vh_1101)/(Rsw(4)) + (Vg_1101-Vout_1101)/(R(9));
eqn6_1101 = (Vf_1101-Vh_1101)/(R(8)) +
(Vg_1101-Vh_1101)/(Rsw(4)) == (Vh_1101-Vout_1101)/(R(10));
eqn7_1101 = (Vg_1101-Vout_1101)/(R(9)) +
(Vh_1101-Vout_1101)/(R(10)) == (Vout_1101)/(PAR.Rload);

```

```

% Solve system of equations
sol_1101 =
solve([eqn1_1101,eqn2_1101,eqn3_1101,eqn4_1101,eqn5_1101,eqn6_1101,
0,eqn7_1101],
[Vc_1101,Vd_1101,Ve_1101,Vf_1101,Vg_1101,Vh_1101,Vout_1101]);

% Outputs for Y
VVout_1101 = sol_1101.Vout_1101;
Iout_1101 = VVout_1101/PAR.Rload;
Req_1101 = (PAR.Vdd - VVout_1101)/Iout_1101;
%-----
%-----
%% SW1=OFF;SW2=OFF;SW3=ON;SW4=OFF;    Vout_1101
; Iout_1101
%-----
%-----

% Node A
% Irl == Isw1 + Ir3;
% Node B
% Ir2 + Isw1 == Ir4;
% Node C
% Ir3 == Isw2 + Ir5;
% Node D
% Ir4 + Isw2 == Ir6;
% Node E
% Ir5 == Isw3 + Ir7;
% Node F
% Ir6 + Isw3 == Ir8;
% Node G
% Ir7 == Isw4 + Ir9;
% Node H
% Ir8 + Isw4 == Ir10;
% Node Vout
% Ir9 + Ir10 == Irl;

% System of equations
syms Va_1111 Vb_1111 Vc_1111 Vd_1111 Ve_1111 Vf_1111 Vg_1111
Vh_1111 Vout_1111
eqn1_1111 = (PAR.Vdd-Va_1111)/(R(1)) ==
(Va_1111-Vb_1111)/(Rsw(1)) + (Va_1111-Vc_1111)/(R(3));
eqn2_1111 = (PAR.Vdd-Vb_1111)/(R(2)) +
(Va_1111-Vb_1111)/(Rsw(1)) == (Vb_1111-Vd_1111)/(R(4));
eqn3_1111 = (Va_1111-Vc_1111)/(R(3)) ==
(Vc_1111-Vd_1111)/(Rsw(2)) + (Vc_1111-Ve_1111)/(R(5));
eqn4_1111 = (Vb_1111-Vd_1111)/(R(4)) +
(Vc_1111-Vd_1111)/(Rsw(2)) == (Vd_1111-Vf_1111)/(R(6));
eqn5_1111 = (Vc_1111-Ve_1111)/(R(5)) ==
(Ve_1111-Vf_1111)/(Rsw(3)) + (Ve_1111-Vg_1111)/(R(7));
eqn6_1111 = (Vd_1111-Vf_1111)/(R(6)) +
(Ve_1111-Vf_1111)/(Rsw(3)) == (Vf_1111-Vh_1111)/(R(8));
eqn7_1111 = (Ve_1111-Vg_1111)/(R(7)) ==
(Vg_1111-Vh_1111)/(Rsw(4)) + (Vg_1111-Vout_1111)/(R(9));
eqn8_1111 = (Vf_1111-Vh_1111)/(R(8)) +
(Vg_1111-Vh_1111)/(Rsw(4)) == (Vh_1111-Vout_1111)/(R(10));
eqn9_1111 = (Vg_1111-Vout_1111)/(R(9)) +
(Vh_1111-Vout_1111)/(R(10)) == (Vout_1111)/(PAR.Rload);

% Solve system of equations
sol_1111 =
solve([eqn1_1111,eqn2_1111,eqn3_1111,eqn4_1111,eqn5_1111,eqn6_1111,
eqn7_1111,eqn8_1111,eqn9_1111],
[Va_1111,Vb_1111,Vc_1111,Vd_1111,Ve_1111,Vf_1111,Vg_1111,Vh_1111,Vout_1111]);

```

```

% Outputs for Y
VVout_111 = sol_111.Vout_111;
Ihout_111 = VVout_111/PAR.Rload;
Req_111 = (PAR.Vdd - VVout_111)/Ihout_111;
%-----
%-----
%%% Output Data

%Y= Vout , Iout , Req
Y = [VVout_0000,Ihout_0000,Req_0000;
     VVout_0001,Ihout_0001,Req_0001;
     VVout_0010,Ihout_0010,Req_0010;
     VVout_0011,Ihout_0011,Req_0011;
     VVout_0100,Ihout_0100,Req_0100;
     VVout_0101,Ihout_0101,Req_0101;
     VVout_0110,Ihout_0110,Req_0110;
     VVout_0111,Ihout_0111,Req_0111;
     VVout_1000,Ihout_1000,Req_1000;
     VVout_1001,Ihout_1001,Req_1001;
     VVout_1010,Ihout_1010,Req_1010;
     VVout_1011,Ihout_1011,Req_1011;
     VVout_1100,Ihout_1100,Req_1100;
     VVout_1101,Ihout_1101,Req_1101;
     VVout_1110,Ihout_1110,Req_1110;
     VVout_1111,Ihout_1111,Req_1111];

end

%%% Trim Function
%-----
%-----
function [TrimPerf] = LadderPerformance(LadderData,PAR)

Trim_0000 = PAR.Rtotal - LadderData(1,3);
Trim_0001 = PAR.Rtotal - LadderData(2,3);
Trim_0010 = PAR.Rtotal - LadderData(3,3);
Trim_0011 = PAR.Rtotal - LadderData(4,3);
Trim_0100 = PAR.Rtotal - LadderData(5,3);
Trim_0101 = PAR.Rtotal - LadderData(6,3);
Trim_0110 = PAR.Rtotal - LadderData(7,3);
Trim_0111 = PAR.Rtotal - LadderData(8,3);
Trim_1000 = PAR.Rtotal - LadderData(9,3);
Trim_1001 = PAR.Rtotal - LadderData(10,3);
Trim_1010 = PAR.Rtotal - LadderData(11,3);
Trim_1011 = PAR.Rtotal - LadderData(12,3);
Trim_1100 = PAR.Rtotal - LadderData(13,3);
Trim_1101 = PAR.Rtotal - LadderData(14,3);
Trim_1110 = PAR.Rtotal - LadderData(15,3);
Trim_1111 = PAR.Rtotal - LadderData(16,3);

TrimChg_0000 = 0;
TrimChg_0001 = Trim_0001 - Trim_0000;
TrimChg_0010 = Trim_0010 - Trim_0001;
TrimChg_0011 = Trim_0011 - Trim_0010;
TrimChg_0100 = Trim_0100 - Trim_0010;
TrimChg_0101 = Trim_0101 - Trim_0100;
TrimChg_0110 = Trim_0110 - Trim_0101;
TrimChg_0111 = Trim_0111 - Trim_0110;
TrimChg_1000 = Trim_1000 - Trim_0110;
TrimChg_1001 = Trim_1001 - Trim_1000;
TrimChg_1010 = Trim_1010 - Trim_1001;
TrimChg_1011 = Trim_1011 - Trim_1010;
TrimChg_1100 = Trim_1100 - Trim_1011;
TrimChg_1101 = Trim_1101 - Trim_1100;
TrimChg_1110 = Trim_1110 - Trim_1101;
TrimChg_1111 = Trim_1111 - Trim_1110;

TrimPerc_0000 = Trim_0000/PAR.Rtotal*100;
TrimPerc_0001 = Trim_0001/PAR.Rtotal*100;
TrimPerc_0010 = Trim_0010/PAR.Rtotal*100;
TrimPerc_0011 = Trim_0011/PAR.Rtotal*100;
TrimPerc_0100 = Trim_0100/PAR.Rtotal*100;
TrimPerc_0101 = Trim_0101/PAR.Rtotal*100;
TrimPerc_0110 = Trim_0110/PAR.Rtotal*100;
TrimPerc_0111 = Trim_0111/PAR.Rtotal*100;
TrimPerc_1000 = Trim_1000/PAR.Rtotal*100;
TrimPerc_1001 = Trim_1001/PAR.Rtotal*100;
TrimPerc_1010 = Trim_1010/PAR.Rtotal*100;
TrimPerc_1011 = Trim_1011/PAR.Rtotal*100;
TrimPerc_1100 = Trim_1100/PAR.Rtotal*100;
TrimPerc_1101 = Trim_1101/PAR.Rtotal*100;
TrimPerc_1110 = Trim_1110/PAR.Rtotal*100;
TrimPerc_1111 = Trim_1111/PAR.Rtotal*100;

% TrimPerf = Ohms , % ,trim change
TrimPerf = [0000,Trim_0000,1/16*000
,TrimPerc_0000,TrimChg_0000;
           0001,Trim_0001,1/16*100 ,TrimPerc_0001,TrimChg_0001;
           0010,Trim_0010,1/16*200
,TrimPerc_0010,TrimChg_0010;
           0011,Trim_0011,1/16*300 ,TrimPerc_0011,TrimChg_0011;
           0100,Trim_0100,1/16*400
,TrimPerc_0100,TrimChg_0100;
           0101,Trim_0101,1/16*500 ,TrimPerc_0101,TrimChg_0101;
           0110,Trim_0110,1/16*600 ,TrimPerc_0110,TrimChg_0110;
           0111,Trim_0111,1/16*700 ,TrimPerc_0111,TrimChg_0111;
           1000,Trim_1000,1/16*800
,TrimPerc_1000,TrimChg_1000;
           1001,Trim_1001,1/16*900 ,TrimPerc_1001,TrimChg_1001;
           1010,Trim_1010,1/16*1000,TrimPerc_1010,TrimChg_1010;
           1011,Trim_1011,1/16*1100,TrimPerc_1011,TrimChg_1011;
           1100,Trim_1100,1/16*1200,TrimPerc_1100,TrimChg_1100;
           1101,Trim_1101,1/16*1300,TrimPerc_1101,TrimChg_1101;
           1110,Trim_1110,1/16*1400,TrimPerc_1110,TrimChg_1110;
           1111,Trim_1111,1/16*1500,TrimPerc_1111,TrimChg_1111];

end

```