Digitally Controlled Trimmable Resistor

DESIGN DOCUMENT

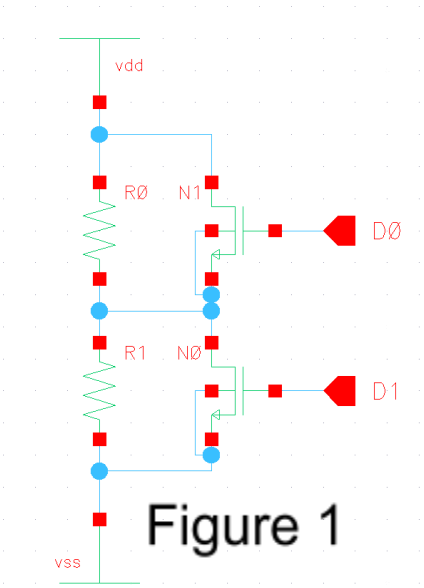

Figure 1

Team Number: 8

Client: Prof. Randy Geiger
Advisers: Prof. Randy Geiger

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Clark Reimers - Test Engineer
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Executive Summary

Development Standards & Practices Used

- IEEE - Follow all IEEE codes of ethics and designing standards for integrated circuits.
- Virtuoso - Follow all virtuoso rules when designing the circuit schematic, layout and running simulation.
- TSMC Process Parameters - Follow process parameters provided by TSMC to make the circuit simulatable and manufacturable.
- Design Flow - Follow a design flow methodology presented in class in order to organize our projects progress. This includes Empathy, Define, Ideate, Prototype, and Test.

Summary of Requirements

- Make a device in .18u CMOS process with adjustable resistance
- Make the resistor highly accurate with a 1% trim
- Size the layout of the circuit to compete with trimmable resistors currently available
- Minimize temperature dependencies within the design
- Manage process variations issues within the design and layout of the circuit
- Be able to adjust the resistance with a discrete input

Applicable Courses from Iowa State University Curriculum

- EE 201 - This course provides the background on relevant passive components that will be used in our design. It also gives us some of the mathematical tools necessary to work with analyzing passive components.
- EE 230- This course covers operational amplifiers. These devices will be used in our simulations.
- EE 330- Gives background knowledge on semiconductor devices like MOSFETs which is a dominant component for the operation of a digitally controllable circuit. This course also teaches us how to do physical layout of an IC.
- CPR E 281- Gives us the digital background for our digitally controlled trimmable resistor. Encoders, decoders, and other digital logic that we will use in our design was learned here.

- MATH 267- Differential equations gives us many analysis techniques that are applicable with circuitry. This course is a foundation for the development of our op-amps.
- EE 332- Physics of semiconductors. This course is extremely in depth into the characteristics of the materials used to create the switches (mosfets) used in this project design.
- LIB 160- This course provides a solid understanding of information literacy and the research process. Since most of our project is research, LIB 160 allowed us to discover many web resources for our research via the use of library discovery tools.
- EE 394- This course helped us to discover the importance of ethics in everything we do.
- ENGL 314- While making our way through this project, we will need to do a lot of documentation. English 314 taught us how to successfully communicate technical information to a specific target audience.

New Skills/Knowledge acquired that was not taught in courses

- Research - Although we discussed resources for research in LIB 160, we have not actually had any courses that focused on pure research.
- Website management- We are a group of mostly electrical engineers with the exception of one computer engineer. This being the case, we have not really dealt with using/designing/managing websites up until this point.
- Several tools and resources- We have learned about the existence of different tools and resources that have been helpful for our progress so far and will continue to be helpful down the road.

Table of Contents

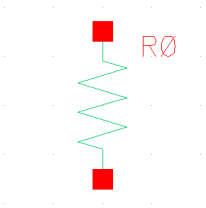
List of figures/tables/symbols/definitions

Definitions:

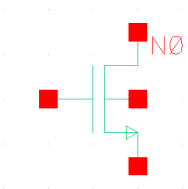
EE	- Electrical engineering
CPR E	- Computer engineering
IC	- Integrated circuit
MOSFET	- Metal oxide semiconductor field effect transistor
PCB	- Printed circuit board
CMOS	- Complementary metal oxide semiconductor
.18u	- CMOS process
PPM	- Parts per million
TCR	- Temperature coefficient of resistance
Cadence	- Company that created Virtuoso
Virtuoso	- Circuit schematic design software
Spectre	- Simulation environment within Virtuoso
N-MOS	- N-type channel MOSFET
Unit Cell	- Circuit design used as building block for other circuit designs

Figures:

Symbols:



Resistor



NMOS transistor

1 Introduction

1.1 Acknowledgement

A big thanks to Randy Geiger for his technical advice throughout our project.

1.2 Problem and Project Statement

Currently in industry, there is a need to modify resistance values for resistors that have been implemented into a working circuit design. There is a way to trim resistors with the use of laser cutting of the resistor film to finely set the desired resistance value. This has the disadvantage of being expensive as well as impossible to do once the IC has been packaged. Also, it is a one-time process that only allows the resistor to be trimmed once. Another solution is with a digital potentiometer using a series, parallel, or ladder resistor structures. This digital solution has low-resolution trimming capabilities with either poor temperature coefficients or physically large components.

This project aims to create a high-resolution digitally trimmable resistor that will fix many of the current solutions. This device will be able to set different resistor values using a digital input that can be finely tuned to different resistance values within a set range. The focus of the project is to improve an architecture based on resistors and switches; the goal is to construct a digitally trimmable resistor that has a high resolution with good temperature coefficients.

1.3 Operational Environment

There are no specific plans for the operational environment of the IC. Conditions such as dust and rain could be mitigated through a device enclosure. Since one of the goals is to minimize the temperature dependencies on the MOSFETs and resistors, extreme temperatures should not be an issue. As such, the design can be utilized in most conditions.

1.4 Requirements

This device requires a resistor that can be repeatedly trimmed over many iterations. The resistor should be modifiable by around 1% per step. This device will require the use of a decoder to set the digital inputs necessary to select a resistance value. It will require a PCB to interface with the device. Lastly, temperature dependencies must be minimized.

1.5 Intended Users and Uses

A digitally controlled trimmable resistor could be used in applications that require an initial calibration, where certain parameters may need to be altered. One example is in an amplifier where the gain needs to be precisely set. Another example of where a trimmable resistor is used is in a cardiac pacemaker. Electrical parameters in this type of environment need to operate within small margins.

1.6 Assumptions and Limitations

Assumptions:

Resistors and MOSFET devices are very temperature dependent by nature. In addition, process variations will exist with all circuits once manufactured. Only resistors and MOSFETS will be used, and the circuit should be re-trimmable many times.

Limitations:

The overall size of the resistors and the switches will need to be small. The trimming should be at a resolution of 1% per step. The temperature coefficient should be at or less than beta ppm/°C.

1.7 Expected End Product and Deliverables

For this project, the expected deliverable is a new method for a digitally controlled trimmable resistor, as opposed to what is currently being used. The design will be within the limitations provided. After coming up with a new approach and the appropriate measurements, the circuit would be simulated using the .18u CMOS process. The end goal is to get a simulation of a device that will meet the constraints set by the client. No physical deliverable is required.

2. Specifications and Analysis

2.1 Proposed Approach

Current Progress:

Current progress has been focused on doing research. In order to design a functional circuit that meets the constraints of the client, it is important that the components used are fully understood. The next step in the process is to look at patents for trimmable resistors to gain more insight. Research has uncovered some interesting approaches to solving the problem for the task at hand and some important uses have been found for the approaches. After learning about some approaches that could be useful for our problem, initial designs have been drafted that could work to meet the end goal. Next the testing phase was initiated. The first focus of design optimization was to the TCR. Progress has been made by doing research on polysilicon temperature characteristics. In order to design a functional circuit that meets the constraints of the client, it is important that the components used are fully understood and that the simulations are running correctly. The next step in the process was to verify that the resistor is being simulated correctly for a given temperature coefficient. Once the resistor is behaving correctly, the MOSFETs will need to be looked at in order to verify that the simulation results are correct. Further on down the road, unit cells will be made out of the resistors and MOSFETs that were previously tested.

Approaches:

The proposed approach includes extensive research in applicable areas of integrated circuits. Gathering and evaluating previous work and literature to learn about current industry standards and designs. These designs should be recreated in order to simulate them as reference designs. Revision and ideation of researched designs as well as brainstormed potential designs should be discussed and then designed. Simulations should be run to test various parameters of interest. Evaluation of the ability to meet requirements specified will be conducted on the specified simulations. After evaluations, the initial design is produced into the modeling software and tested in comparison to the test designs. The approach has not been modified, but is subject to change in the future as new information is uncovered and can be applied to the design. Ultimately work will be done to create potential designs that have promise to be an improvement of the stated shortcomings of current industry designs.

Standards:

Relevancy to standards falls heavily under the IEEE code of ethics. As research is conducted on current industry practices, credit will be given according to contributions in the design where applicable. Another standard for this project is

the CMOS process that is selected for circuits that are designed. The .18 CMOS process will be used as a constant process for all of the designs. Since the end goal is a simulated circuit, other standards are not anticipated as relevant to this project.

2.2 Design Analysis

Initial methods tested include the series resistor design, and the parallel resistor design. These approaches have been modeled in Virtuoso and tested in order to examine the trimming resolution and temperature coefficient properties. Examples include the series design which has a major flaw due to the current path flowing through MOSFETs, when current flows through the MOSFET, temperature variables affect the performance. Also, the parallel designs' flaw shows up in the physical size of the IC due to the resistors being in parallel. Overall the analysis should show the ability of the design's resolution capabilities and temperature stability.

2.3 Development Process

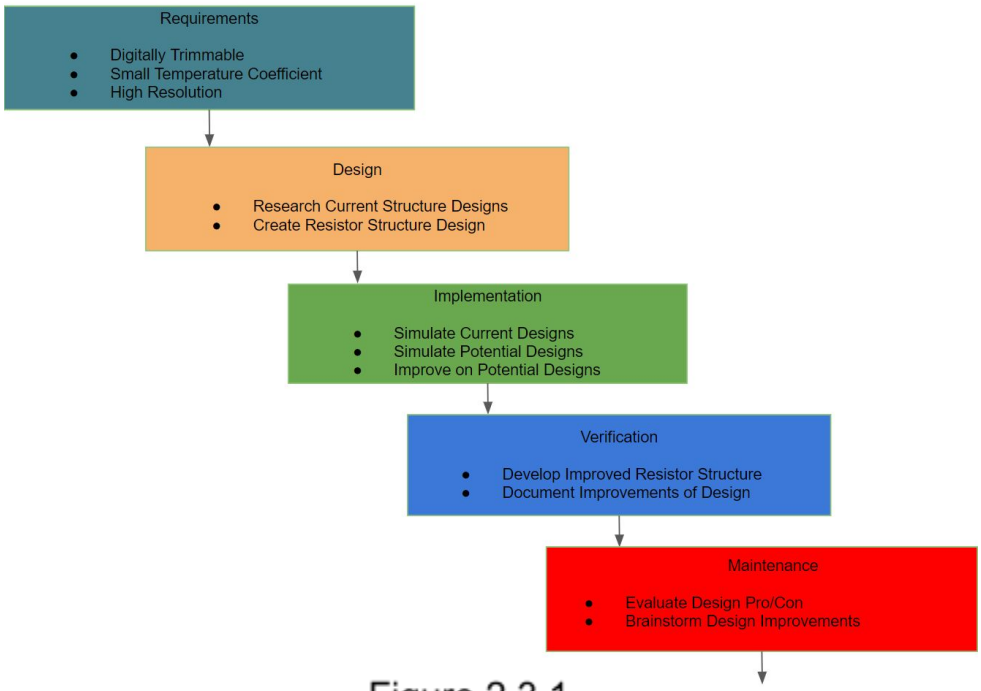


Figure 2.3.1

For this project, a waterfall development process is being followed. A lot of time has been spent in the requirements phase to study the effects of different current solutions in industry and find what constraints that will be selected for our design. Research has been conducted on simpler approaches to the resistor structure.

Many test designs have been implemented into Cadence Virtuoso to be compared with the initial design. This can be used as a more in depth form of researching for the first design step. Multiple initial designs have been drafted as potential approaches to a more concrete design. An initial design has been implemented into Virtuoso in order to compare our other designs to a reference. New potential designs have been designed and simulated to evaluate their potential for a final design.

2.4 Conceptual Sketch

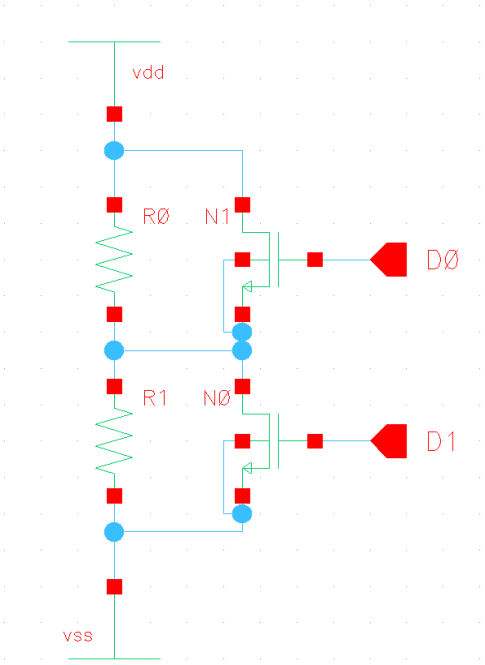


Figure 2.4.1

The initial intuition for a trimmable resistor design is to put resistors in series out to the N^{th}, and then put switches in parallel to a respective resistor. With an encoder, the gates on the switches can be set to high or low resulting in the switches opening or closing. When a switch is closed, ideally, an electrical short beside the resistor will occur which essentially will allow current to completely bypass the resistor. This allows for trimming of the overall resistor unit cell. When driving current through a MOSFET, temperature variations are unfortunately introduced. This is a big performance issue due to breaking the voltage divider ratio by introducing new temperature dependencies.

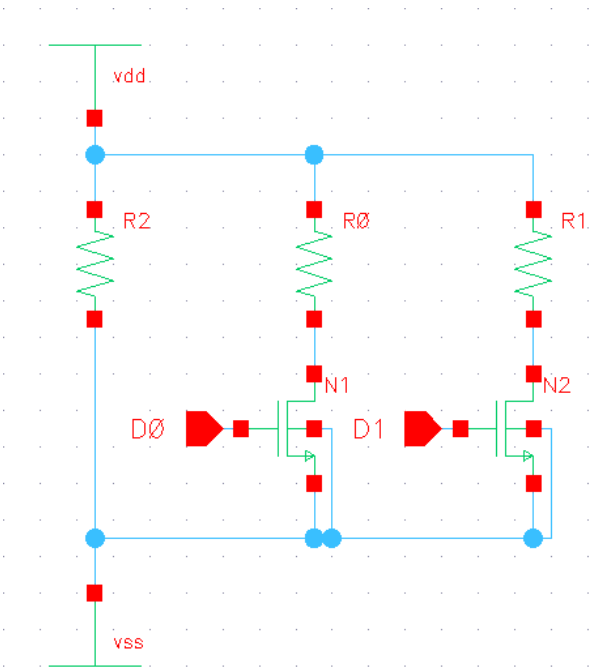


Figure 2.4.2

Another approach discussed was positioning the resistors in parallel which would result in the MOSFETS to be in series with the resistors. When a switch is open, current does not flow through the respective path; therefore, that path does not interact with the performance of the unit cell. When a switch is closed, current flows through the resistor which in turn will affect the performance of the unit cell. Unfortunately resistors in parallel are added by taking the inverse of the resistor value, so with a parallel resistor design the resistors become exponentially large. This negatively impacts the physical size of the design.

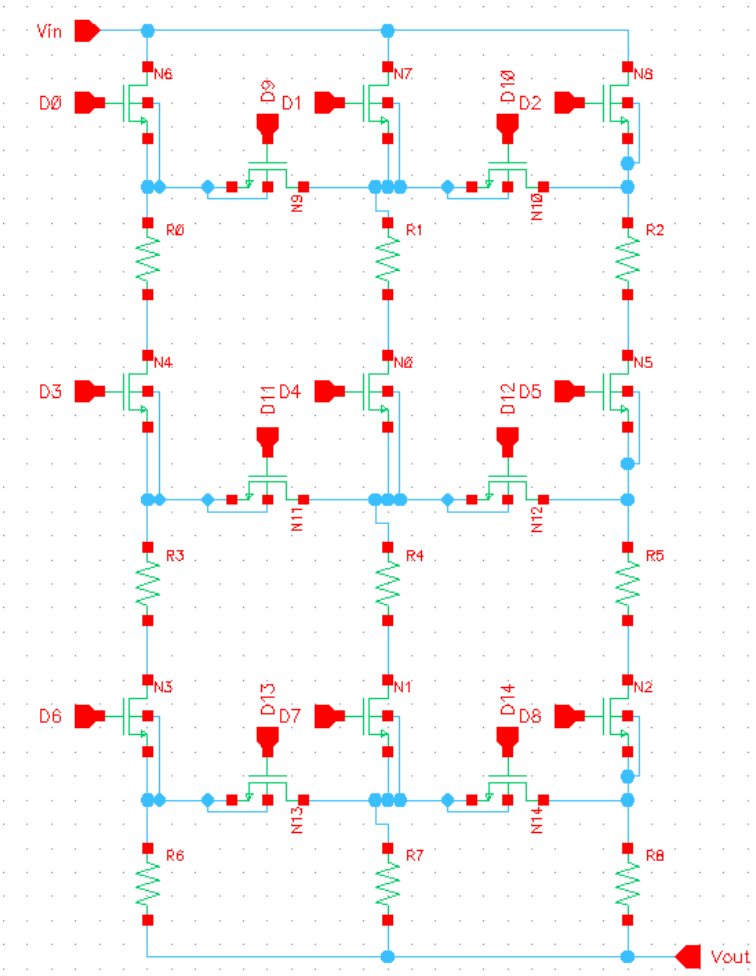


Figure 2.4.3

After looking at a series and parallel approach to trimming a resistor, the idea of combining them was approached. By combining the two designs previously discussed we hope to mitigate the negative effects each of the designs have. Figure 2.4.3 shows a matrix of resistors that have resistors in series and parallel. Then by using switches between the paths we are able to control the flow of current through the matrix of resistors. This then results in a trimmable resistor with the negative effects being mitigated in the process.

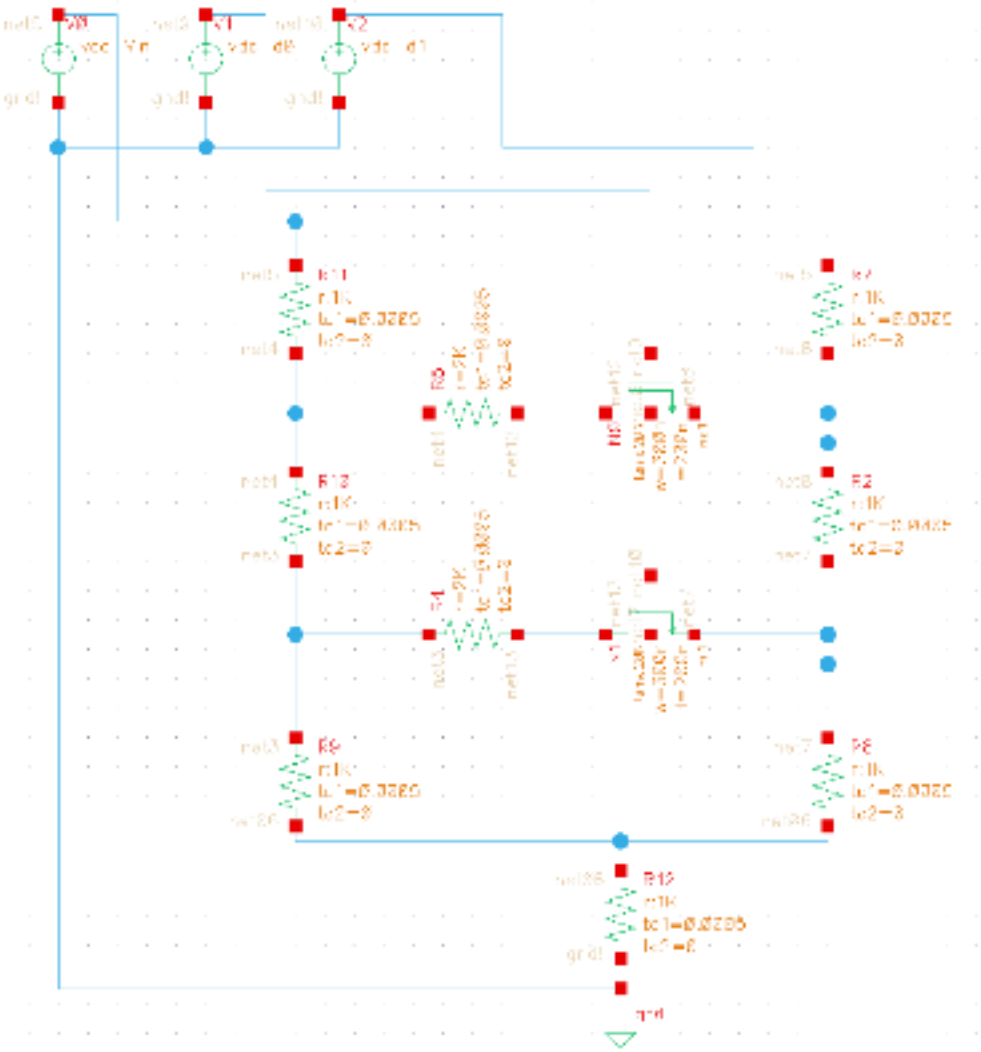


Figure 2.4.4

A design that has been adopted as of recently is the ladder structure. This design is advantageous because of its ability to avoid TCR effects very well. The idea of this design is to ensure that the current avoids flowing through the MOSFET devices. Both the on/off states of the switch will ideally have the same TCR effects.

3. Statement of Work

3.1 Previous Work And Literature

The first work of relevant literature for information on this project's topics is “The Art of Analog Layout”, by Alan Hastings [1]. A second piece of literature relevant to the work on this project is the textbook Analog Integrated Circuit Design by T. C. Carusone, K. W. Martin, and D. Johnsby [2]. Another good resource on this topic is the book Microelectronic Circuits by A. S. Sedra and K. C. Smith [3].

The previous work of this type of trimming has been used in many applications requiring the ability to precisely trim a chip after manufacturing where laser trimming is not applicable. Documentation of previous work includes a patent by Cardiac Pacemakers Inc, where digitally trimmable resistors were used for bandgap voltage reference [4]. This method used a series resistor structure which has been simulated as one of our reference designs. This design has the shortcoming of having a poor temperature coefficient due to the large amount of current flowing through the switches.

Another popular method for trimmable resistors is the ladder structure. In a patent invented by Jimmy R. Naylor, a R/2R Ladder structure of resistors was implemented in order to create a new method for digital to analog converters[5]. This ladder structure is a promising resistor structure because of its improvement on both the series and parallel approaches. This is the primary structure that our project will be focusing on improving.

Other methods of trimmable resistors include the patent Dual thin film precision resistance trimming by STMicroelectronics Inc [6]. This design implements a heater on the IC that can precisely control the temperature of the resistors. This utilizes the temperature coefficient properties to modify the resistance values and achieve a fine resistor trim. A drawback of using an on-chip heater is the amount of space that will be required to do so. Space is part of the project requirement and therefore the heater is not something that can be utilized. It also takes a lot of power to use an on-chip heater, which is another drawback of this approach.

To focus on the digital trim, other sources have been used as resources to further improve the trimming designs. Utilizing the textbook and lecture material from our academic advisor, Dr. Geiger was a crucial part as a starting point in TCR optimization [7]. One paper from the Journal of Applied Physics, titled “The electrical properties of polycrystalline silicon films” allowed us to get a more in depth correlation to the temperature characteristics of the resistors in the process selected [7].

3.2 Technology Considerations

The project will rely heavily on MOSFET technology as switches in the trimmable resistor. Current MOSFET technologies do have a few weaknesses, however. The major one is the non-linearity performance due to temperature effects. If the switches were ideal, then the performance degradation caused by temperature effects would not be an issue. Unfortunately, these effects are a genuine issue throughout this project, but there are a few solutions to this issue. One such solution is to limit the amount of current flowing through the MOSFET to reduce the adverse effects. The tradeoff of doing this will be the need for more switches in the circuit. Solutions to the temperature effects could result in a tradeoff. The pros and cons of each solution will need evaluating to ensure that the solution is a valid one.

In addition, there will be a tradeoff with the physical size of the circuit and the accuracy. As a focus on accuracy becomes a dominant player in our design, the circuit will become much larger; therefore, our team will need to define what an acceptable physical size of the circuit is and then pack as much accuracy into the circuit given the circuit size limitation.

3.3 Task Decomposition

In order to successfully complete the digitally programmable trimmable resistor, our team broke up the project into multiple tasks.

1) Meet with our advisor to discuss technical goals, progress, and to make changes as needed.
2) Research existing designs and review our fundamentals.
3) Ideate and discuss ideas our team brainstormed.
4) Simulate reference design and acquire temperature coefficient.
5) Simulate our designs and compare them to the reference design performance.
6) Pick the most promising design based on performance characteristics and hone it into a finished product.
7) Prepare presentation and documentation.

Above are the tasks that will help our team stay on track to finishing the project.

3.4 Possible Risks And Risk Management

One major hindrance to the success of our project is access to the virtuoso software needed in order to design and simulate potential circuits. Some reasons that might make it difficult to access Virtuoso would be remote desktop issues, vpn issues and lab room closures. Additionally, there may be times when team members will have issues with their internet access.

Another roadblock that might come up is simulation issues due to novice knowledge on the proper way to perform simulations within Virtuoso. Our team is going to rely heavily on the simulation results to determine the performance of circuit designs, but if simulation issues present themselves, then our team will need to remove this road block before any more progress can be made.

Lastly, when it comes to circuit design, there are a lot of nuances and rules that need to be understood in order to successfully get a circuit to behave properly. During the project, it might become more apparent that our team's knowledge on the general operations and behavior of circuits might be lacking and require extra time to develop and evaluate the circuit designs.

3.5 Project Proposed Milestones and Evaluation Criteria

Over the course of our projects progress, there are a few milestones that will need to be hit. Below lists a few of the milestones that our team will work towards reaching.

1) Measure the temperature coefficient of a resistor.
2) Measure the temperature coefficient of a MOSFET.
3) Measure the temperature coefficient of a series trimmable resistor structure.
4) Pick one final circuit design to complete our project with.

By performing well established simulations, we should be able to confirm proper operation of the design. If there are any questions regarding the accuracy of any results, they can be directed to the faculty advisor. The faculty advisor is an expert in the area and should be able to provide us with meaningful and reliable guidance.

3.6 Project Tracking Procedures

We have decided to use Trello to keep track of progress and goals throughout the project. We are also utilizing Google Drive since we lack the knowledge of easy

collaboration with Virtuoso. Google Drive allows us to share created content with other team members so that it can be improved upon. It also documents any completed assignments and important resources. Other methods of project tracking include recording online meetings with Google Meet for documenting project checklist items, documenting updates within Google Slides for tracking presentable progress, and Microsoft Sharepoint for documenting data collection and calculation.

3.7 Expected Results and Validation

The desired outcome is to design a digitally controllable trimmable resistor. This trimmable resistor will need to have high accuracy and resolution, as well as low temperature dependencies in order to make it compete with current designs in the market.

For high level verification of the final design, our team will be using simulation environments in Virtuoso. The simulation results generated will be a direct reflection on the performance of the design.

4. Project Timeline, Estimated Resources, and Challenges

4.1 Project Timeline

sddec20-08 Gantt chart

Figure 4.1.1

The plan is to have the work split up between two semesters, using the first semester mostly for research, administration, and ideation. The first half should lay proper groundwork leading into the second half of the project. The focus in the second half will be choosing specific designs that show promise and refining them. The end goal will be to create a design that meets the project requirements. The focus will then shift to preparing documentation and running proper tests to confirm everything is accurate. Finally, we will present our findings to an industry panel along with the documentation that was developed, proving that the design meets the project requirements.

4.2 Feasibility Assessment

This project will consist of researching current methodologies of resistor trimming technologies. The goal will be to improve upon current technologies and develop a new resistor concept that garners interest as a useful product in the electronics community. In particular, the product will be a high-resolution digitally trimmable resistor that has no temperature dependencies. The challenges associated with this project are mostly that of the feasibility variety. It is not yet known if such a product can be developed. Research and development in this area requires specialization of the topic. Another challenge that could be encountered are simulation results that may not quite align with reality. Simulation results could also be subject to misinterpretation.

4.3 Personnel Effort Requirements

Task	Time/Person
Administrative	30 hrs
Research	60 hrs
Ideate	30 hrs
Simulate	40 hrs
Development	80 hrs
Documentation/Presentation	40 hrs

Table 4.3.1

4.4 Other Resource Requirements

The materials needed for this project are as follows:

- Computers for each team member
- Internet connection for each team member
- Communication software
- Simulation software

All of these materials are accessible by each member with no extra associated costs.

4.5 Financial Requirements

There are no anticipated financial resources required to conduct the project. Everything will be digitally designed and simulated. All resources for this have been provided by Iowa State University at no cost. There is a possibility for fabrication of the final design but that is not something that is anticipated at this current time.

5. Testing and Implementation

Fundamentally the project is made up of 3 parts:

- Research
- Ideation
- Testing

The first step was researching concepts and ideas that can be used in the designs. The next step is to come up with circuits that encompass the research results to meet the goal. Then, the circuits are tested to ensure that the test results are as expected and meet the required goals. Testing is a key component as it allows the designer to evaluate their ideas. This gives them the ability to choose a final design that has the best performance relative to the goal. Because testing is so important, it is important that all of the tests are true and complete. Validity of a circuit as a product cannot be determined if the test that is used to validate it is wrong or inadequate.

All of the design work is done in Cadence Virtuoso, and the testing is done through Cadence Spectre within Virtuoso. For each circuit design, the following tests are needed:

- Temperature coefficient
- Scalability (can we go from a 1-cell design to an n-cell design)
- Resolution of the trimmable resistor
- Reproducibility of expected results (can we re-trim the device over and over again)

The individual items to be tested are as follows:

- Resistor
- N-MOS MOSFET

The individual designs above will be tested to ensure the simulation environment is behaving correctly and the component parameters are correct.

To determine the resolution and the range of the trimmable resistor, a sweep through all possible state combinations of the switches will be performed. To test the scalability of the design, one unit cell will be created and tested in a test bench to ensure proper functionality. To check the expansion of the design, more unit cells will be cascaded into the test bench and make sure the functionality is still achieved. Reproducibility of the device will be determined by repeatedly running tests and verifying that the resulting output is the same as the first test run(within a specified tolerance). Finally, to check the temperature coefficient of the design, a

dc sweep ranging from 0 to 100 degrees celsius will be created. The input voltage and input current will be plotted afterwards. Once plotted, Microsoft Excel will be used to calculate the temperature coefficient values per sweep step.

The anticipated test results for the temperature coefficient of the designed circuit is ideally zero. A temperature coefficient of zero may not be possible, so the goal will be to get it as close to zero as possible. Scalability of the circuit will be determined by whether or not the goal has been met. It is expected that an individual cell should function such that adding more cells to it will meet the goal of the overall circuit. If the cells cannot be cascaded until the goal is met, the circuit is not scalable. Resolution of the resistor needs to be high. The goal is ±1%. Reproducibility will ideally be infinite, but there will be physical limitations when the circuit is brought into the real world. Simulation results of the circuit are expected to be reproducible 100 times once it passes initial testing for other requirements.

5.1 Interface Specifications

All testing interface tools will come from Cadence Virtuoso and the Cadence Spectre simulation environment.

5.2 Hardware and software

All testing and simulating is done using Virtuoso and the Spectre toolkit included in it. Many tests are performed using dc sweeps across temperature. This is useful because it will perform the simulation over a range which would take a lot of time by hand to do. Microsoft Excel is used to break down the plots generated by Virtuoso to better analyze the results.

5.3 Functional Testing

Unit Tests:

Both the resistor and the MOSFET components will be tested to ensure the simulation environment is behaving correctly and the component parameters are correct.

Integration Tests:

Unit cells will be tested in a Virtuoso test bench to make sure the behavior of the unit cell is as expected.

System Tests:

After testing all the unit cells, the unit cells will be combined to increase the resolution and range of the resistor. It will be tested using a transient analysis across all input variables to generate a plot. The plot will be analyzed to ensure proper behavior was observed.

Acceptance Tests:

The overall acceptance test will be completed once the completed circuit is made. Then the test results will be compared to the reference design to determine if any performance characteristics have improved.

5.4 Non-Functional Testing

Testing for Performance:

The trimmable resistor will be tested for performance by cycling all digital input combinations to ensure the trimmable functionality works. Then the trimmability accuracy will be tested by attempting to trim the resistor to an exact value.

Testing for Security:

This is not applicable for a trimmable resistor type project.

Testing for Usability:

The circuit's usability will be tested by making a few test bench applications where a trimmable resistor may be applied. In addition the input voltage range of the circuit will be comparable to other similar trimmable resistors currently on the market .

Testing for Compatibility:

The circuit will be capable of accepting a wide variety of input signals thus making it compatible with most users' applications. To test for this, the circuit will be tested in a test bench test environment.

5.5 Process

Various simulations will be carried out to ensure the components are being used in their appropriate environment and that the resolution is high enough, this would require some trial and error. Microsoft Excel has the ability to import the results from Spectre and allows a better analysis of the data.

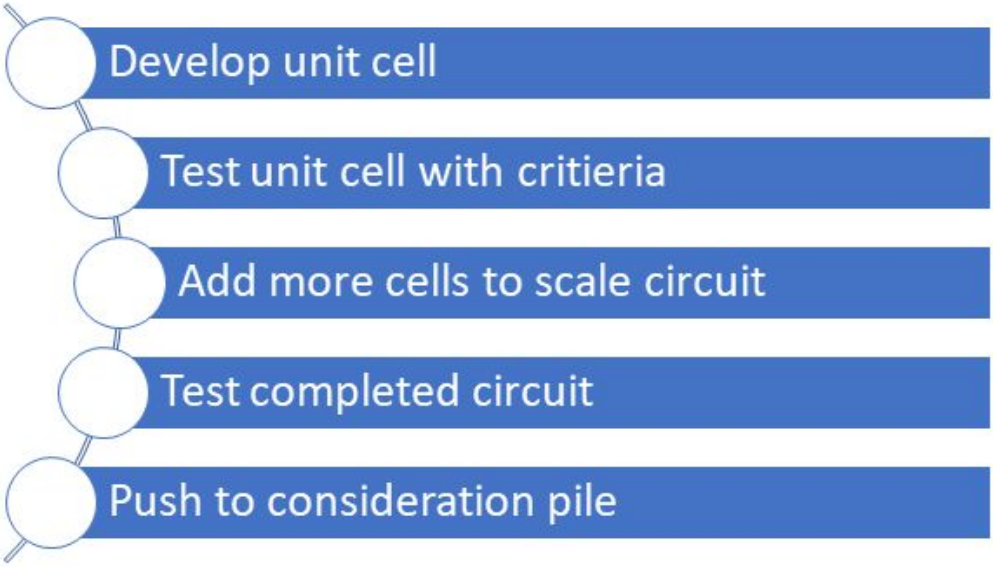


Figure 5.5.1

5.6 Results

The initial test performed was to get a basic series trimmable resistor circuit(figure 2.4.1) to run that way we could have this reference circuit to compare with our final product.

During the testing phase, there was one issue that took the front stage; how Virtuoso handles temperature coefficients. Due to the nature of integrated circuits, getting the correct behavior for temperature characteristics is key. To overcome this issue, research in polysilicon temperature characteristics resulted in finding polysilicon conductivity.

The first approach we took was having a constant TCR. We simulated our circuit with a TCR of 500 ppm/°C which we found from Dr. Geiger's lecture notes. The results from this simulation gave us a linear equation for the TCR of resistance. We realized that our equation for TCR was different from Cadence's equation. This is because Cadence uses an equation that takes a nominal resistance value as a parameter, while our equation uses the temperature value at the temperature where the TCR is being measured.

We realized that the real TCR needed to be discovered through the material properties of polysilicon. We arrived at the idea that the inverse of conductivity is the resistivity. From that discovery, the temperature coefficient equation can be derived from the derivative of resistivity with respect to temperature divided by the resistivity. In addition to the temperature dependence of the equation, the TCR varies depending on the material properties of the polysilicon. Depending on the carrier concentration of the polysilicon, the energy barrier will change resulting in a change in the TCR. An equation was tested in a simple voltage source resistor circuit, and the result is shown in figure 5.6.1. There were many iterations of equations tested with different parameters. A final resistor material

and TCR parameter was found that can be used for our designs. With our new found knowledge, all the future simulations of circuit designs can be run with the proper resistor parameters for our fabrication process.

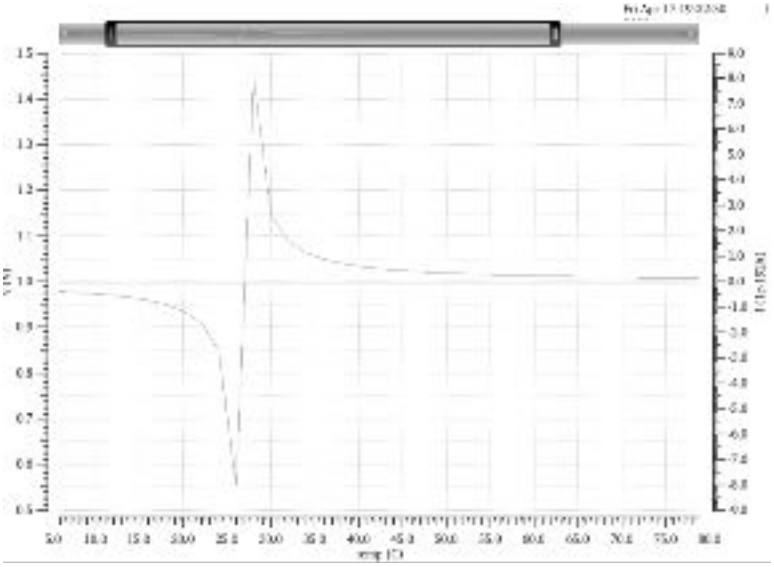


Figure 5.6.1

6. Closing Material

6.1 Conclusion

This semester we have focused primarily on four things:

1. Completely understanding the problem that the client needed a solution for and developing an approach/timeline.
2. Defining and obtaining the essentials needed to complete the project
3. Reviewing engineering fundamentals and researching possible solutions to the task that was given to us. This also includes researching current solutions available on the market to see what went right and what went wrong.
4. Ideate some circuits that could meet the requirements of the project and establish thorough testing.

The goal of our project is to develop a high-resolution digitally trimmable resistor. The resolution of the resistor should be ±1% and the value of the resistance should be controlled by an n-bit boolean input. The reason why this is an important project is due to the numerous applications throughout the semiconductor industry where such a device is needed. There are multiple methods for this device but each method has its own drawback. We want to improve upon the temperature coefficient and the resolution of the currently available circuits to create a new trimmable resistor that is still cheap with a new architecture.

We believe that the best plan of action to achieve our goals is the following:

- Meet with our advisor to discuss technical goals, progress, and to make changes as needed.
- Research existing designs and review our fundamentals.
- Ideate and discuss ideas our team brainstormed.
- Simulate reference designs and acquire their temperature coefficients.
- Simulate our designs and compare them to the reference design performance.
- Pick the most promising design based on performance characteristics and hone it into a finished product.
- Prepare final presentation and documentation.

We cannot say that this plan of action surpasses all others (that would be a rather large assertion), but it is a good plan for the following reasons:

- It is efficient because we start small scale and work our way up (as opposed to trying to handle it all at once and failing)
- It is smart because we take the time to look at other designs to see how they could apply to our particular problem. This reduces unnecessary effort on our part.
- It allows us to establish a good timeline.
- It is a complete plan of action.

6.2 References

[1] A. Hastings, *The art of analog layout*. Upper Saddle River, NJ: Prentice Hall, 2011.

[2] T. C. Carusone, K. W. Martin, and D. Johns, *Analog integrated circuit design, 2nd edition*. Hoboken, NJ: John Wiley & Sons, 2011.

[3] A. S. Sedra and K. C. Smith, *Microelectronic circuits*. New York: Oxford University Press, 2015.

[4]Cardiac Pacemakers, Inc., 2020. *Digitally Trimmable Resistor For Bandgap Voltage Reference*. US6381491B1.

[5] J.R. Naylor, 'R/2r ladder circuit and method for digital-to-analog converter', WO1999026345A1, 1999.

[6] O.L. Neel, P. Dumont-Girard, C. Niu, F. Wang, M. Arnoux, 'Dual thin film precision resistance trimming' US8242876B2, 2012.

[7] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI DESIGN TECHNIQUES FOR ANALOG AND DIGITAL CIRCUITS*.

[8] J. Y. W. Seto, "The electrical properties of polycrystalline silicon films," *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.

6.3 Appendices

Virtuoso for circuit designs (Website PDF Link):
http://home.engineering.iastate.edu/~yulong/EE501lab/Cadence%20analog%20design%20environment%20user%20guide%202006.pdf

Spectre for circuit analysis (Website PDF Link):

http://eece.cu.edu.eg/~fhussien/Spectre_tutorial.pdf

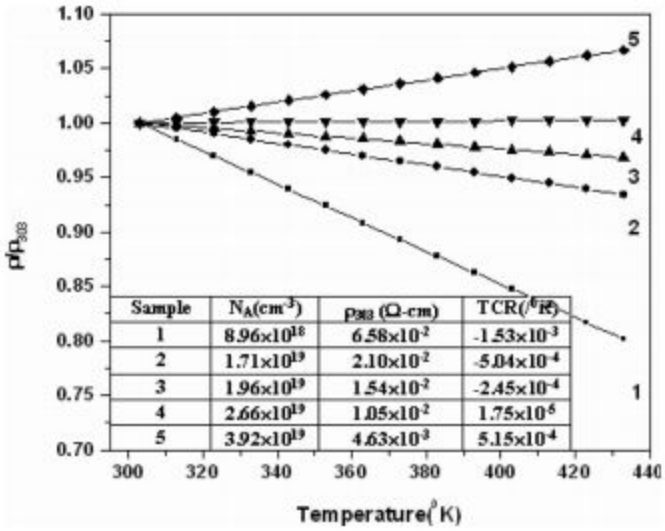


Figure 6.3.1

Normalized resistivity versus temperature for ion-implanted samples

TABLE I. Trapping state density and energy barrier height for three samples with different doping concentrations.

Doping concentration	Energy barrier, E_B	Trapping state density, Q_t
$5\times10^{18}/cm^3$	0.0335 eV	$2.98\times10^{12}/cm^2$
$1\times10^{19}/cm^3$	0.022 eV	$3.41\times10^{12}/cm^2$
$5\times10^{19}/cm^3$	0.005 eV	$3.64\times10^{12}/cm^2$

Figure 6.3.2

Energy barrier and State density for Doping concentrations

Eq. (13) the conductivity of a polysilicon film with a grain size L cm is

$$\sigma = Lq^2 p_a \left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_B}{kT}\right). \tag{14}$$

Inserting Eqs. (6) and (11) into Eq. (14), we find that

$$\sigma \propto \exp[-(\tfrac{1}{2}E_g - E_f)/kT], \quad \text{if } NL < Q_t, \tag{15}$$

$$\sigma \propto T^{-1/2} \exp(-E_B/kT), \quad \text{if } NL > Q_t. \tag{16}$$

Figure 6.3.3
Polysilicon conductivity equations