# Digitally Controlled Trimmable Resistor

DESIGN DOCUMENT

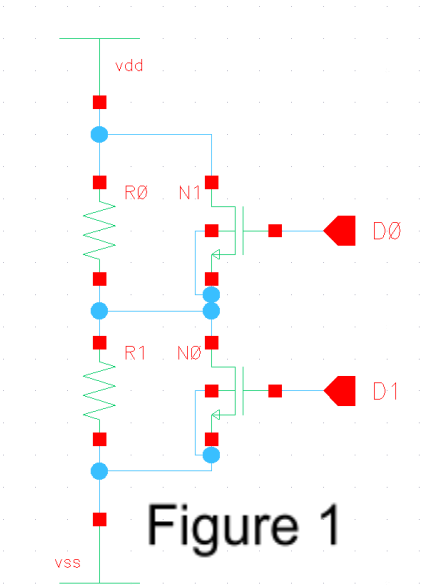


Figure 1

Team Number: 8

Client: Prof. Randy Geiger
Advisers: Prof. Randy Geiger

**Team Members/Roles:**
Clark Reimers - Test Engineer
Pierce Nablo - Design Engineer
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# Executive Summary

## Development Standards & Practices Used

- IEEE - Following all IEEE codes of ethics and designing standards for integrated circuits.
- Virtuoso - Follow all virtuoso rules when designing the circuit schematic, layout and running simulation.
- TSMC Process Parameters - To design our project in virtuoso given process parameters will be followed to make the circuit simulatable and manufacturable.
- Design Flow - Follow a design flow methodology presented in class in order to organize our projects progress. This includes Empathy, Define, Ideate, Prototype, and Test.

## Summary of Requirements

- Make a device in .18u CMOS process with adjustable resistance
- Make the resistor highly accurate with a 1% trim
- Size the layout of the circuit to compete with trimmable resistors currently available
- Minimize temperature dependencies within the design
- Manage process variations issues within the design and layout of the circuit
- Be able to adjust the resistance with a discrete input

## Applicable Courses from Iowa State University Curriculum

- EE 201 - This course provides the background on relevant passive components that will be used in our design. This also gives us some of the mathematical tools necessary to work with analyzing the passive components in our circuit.
- EE 230- This course covers operational amplifiers. These devices will be used in our simulations.
- EE 330- This course provides the background for our semiconductor devices inside of our IC. The most predominant devices of our design will be resistors and MOSFETs. This course also teaches us how to do physical layout of an IC.

- CPR E 281- This gives us the digital background for our digitally controlled trimmable resistor. Encoders, decoders, and other digital logic that we will use in our design was learned here.
- MATH 267- Differential equations gives us many analysis techniques that are applicable with circuitry. This course is a foundation for the development of our op-amps.
- EE 332- Physics of semiconductors. This course is extremely in depth into the characteristics of the materials used to create the switches (mosfets) used in this project design.
- LIB 160- This course provides a solid understanding of information literacy and the research process. Since most of our project is research, LIB 160 allowed us to discover many web resources for our research via the use of library discovery tools.
- EE 394- This course helped us to discover the importance of ethics in everything we do.
- ENGL 314- While making our way through this project, we will need to do a lot of documentation. English 314 taught us how to successfully communicate technical information to a specific target audience.

## New Skills/Knowledge acquired that was not taught in courses

List all new skills/knowledge that your team acquired which was not part of your Iowa State curriculum in order to complete this project.

- Research - Although we discussed resources for research in LIB 160, we have not actually had any courses that focused on pure research.
- Website management- We are a group of mostly electrical engineers with the exception of one computer engineer. This being the case, we have not really dealt with using/designing/managing websites up until this point.
- Several tools and resources- We have learned about the existence of different tools and resources that have been helpful for our progress so far and will continue to be helpful down the road.

# Table of Contents

## List of figures/tables/symbols/definitions (This should be the similar to the project plan)

**Definitions:**

EE - electrical engineering

CPR E - computer engineering

IC- integrated circuit

MOSFET - metal oxide semiconductor field effect transistor

PCB - Printed Circuit Board

.18u CMOS process

**Figures:**

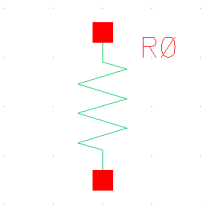
1 - Title Page Picture

2.4.1 - Series Resistor Design

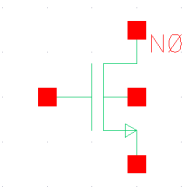
2.4.2 - Parallel Resistor Design

2.4.3 - Matrix Resistor Design

**Symbols:**




Resistor




NMOS transistor

# 1 Introduction

## 1.1 Acknowledgement

A big thanks to Randy Geiger for his technical advice throughout our project.

## 1.2 Problem and Project Statement

Currently in industry, there is a need to modify resistance values for a resistor that has been implemented into a working circuit design. There is a way to do this trimming with the use of laser cutting of the resistor film to finely set the desired resistance value. This has the disadvantage of being expensive as well as impossible to do once the IC has been packaged. Also, It is a one-time process that only allows the resistor to be trimmed once. Another solution is with a digital potentiometer using a series or parallel resistor structure. This solution has low-resolution trimming capabilities with either poor temperature coefficients or physically large components.

This project aims to create a high-resolution digitally trimmable resistor that will fix many of the current solutions to the need for trimmable resistors. This device will be able to set many different resistance values using a digital input that can be finely tuned to different resistor values within a set range. Focusing on improving the architecture based on resistors and switches, the goal is to construct a digitally trimmable resistor that has a high resolution with good temperature coefficients.

## 1.3 Operational Environment

There are no specific plans for the environment of our IC. Conditions such as dust and rain could be mitigated through a device enclosure. Since one of the goals is to minimize the temperature dependencies on the MOSFETs and resistors, extreme temperatures should also not be an issue. As such, the design can be utilized in most conditions.

## 1.4 Requirements

This device requires a resistor that can be repeatedly trimmed over many iterations. It should be able to modify the resistances by around 1% per step. This device will require the use of a decoder to set the digital inputs necessary to select a resistance value. It will require a pcb to house the device in order to resist

current. Another requirement for our project is that it minimizes temperature dependencies.

## 1.5 Intended Users and Uses

A digital trimmable resistor would be used in applications that require an initial calibration, it would allow certain parameters to be altered. An example of where a trimmable resistor would be used is a cardiac pacemaker, that would require the parameter to be changed when called upon.

## 1.6 Assumptions and Limitations

Assumptions: Resistors and MOSFET devices are temperature dependent by nature. There would be process variations, only resistors and mosfets switches would be used, should be able to be trimmed many times.

Limitations: The total value of resistor and size of the switch shouldn't be big. The trimming should be at a resolution of 1% per step. The temperature coefficient should be at or less than beta ppm/°C.

## 1.7 Expected End Product and Deliverables

For this project, the expected deliverable is a new method for a digitally trimmable resistor, as opposed to what is currently being used. The design will be within the limitations provided. After coming up with a new approach and the appropriate measurements, the circuit would be simulated using the .18u CMOS process. The end goal is to get a simulation of a device that will meet the constraints set by the client. No physical deliverable is required.

# 2. Specifications and Analysis

## 2.1 Proposed Approach

Current Progress:

A lot of the current progress has been doing research. In order to design a functional circuit that meets the constraints of the client, it is important that the components used are fully understood. The next step in the process is to look at patents for trimmable resistors to gain more insight. Research has uncovered some neat approaches to solving the problem for the task at hand and some important uses have been found for the approaches. After learning about some approaches that could be useful for our problem, initial designs have been drafted that could work to meet the end goal.

Approaches:

The initial approach was to build on basic understandings, develop some circuits, test, and revise. The approach has not been changed yet but may be done further down the road as new information is uncovered and can be applied to the design. The initial approaches are testing current resistor structures to examine the pros/cons of these designs. Afterwards the initial design is produced into the modeling software and tested in comparison to the test designs.

Standards:

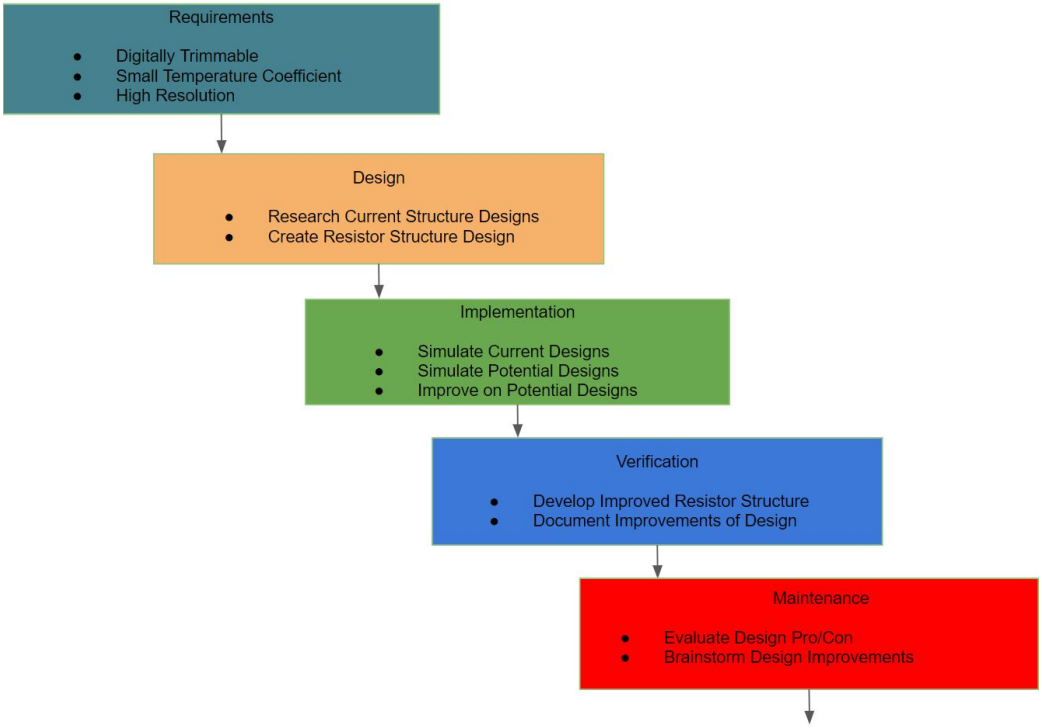
Relevancy to standards falls heavily under the IEEE code of ethics. As research is conducted about current industry practice, credit will be given according to contributions in the design where applicable. Since the end goal is a simulated circuit, other standards are not anticipated as relevant to this project.

The proposed approach includes extensive research in applicable areas of integrated circuits. Gathering and evaluating previous work and literature to learn about current industry standards and designs. These designs should be recreated in order to simulate them as reference designs. Revision and Ideation of researched designs as well as brainstormed potential designs should be discussed and then designed. Simulations should be run to test various parameters of interest. Evaluation of the ability to meet requirements specified will be conducted on the specified simulations. Ultimately work will be done to create many potential designs that have promise to be an improvement of the stated shortcomings of current industry designs.

## 2.2 Design Analysis

Initial methods tested include the series resistor design, and the parallel resistor design. These approaches have been modeled in Virtuoso and tested in order to examine the trimming resolution and temperature coefficient properties. Examples include the series design which has a major flaw due to the current path flowing through MOSFETs, when current flows through the MOSFET, temperature variables affect the performance. Also, the parallel designs' flaw shows up in the physical size of the IC due to the resistors being in parallel. Overall the analysis should show the ability of the design's resolution capabilities and temperature stability.

## 2.3 Development Process




For this project a waterfall development process is being followed. A lot of time has been spent in the requirements phase to study the effects of different current solutions in industry and find what constraints that will be selected for our design. Research has been conducted on simpler approaches to the resistor structure. Many test designs have been implemented into Cadence Virtuoso to be compared with the initial design. This can be used as a more in depth form of researching for the first design step. Multiple initial designs have been drafted as potential approaches to a more concrete design. An initial design has been implemented into Virtuoso in order to compare our other designs to a reference. New potential designs have been designed and simulated to evaluate their potential for a final design.

## 2.4 Conceptual Sketch

The initial intuition for a trimmable resistor design is to put resistors in series out to the $N^{th}$, and then put switches in parallel to a respective resistor. With an encoder, the gates on the switches can be set to high or low resulting in the switches opening or closing. When a switch is closed, ideally, a short beside the resistor will occur which essentially will allow current to completely bypass the resistor. This allows for trimming of the overall resistor unit cell. When driving current through a MOSFET, temperature variations are unfortunately introduced. This is a big performance issue due to breaking the voltage divider ratio by introducing temperature dependencies.

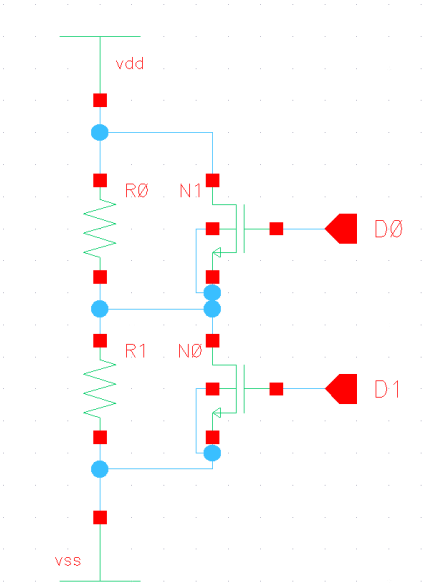



Figure 2.4.1

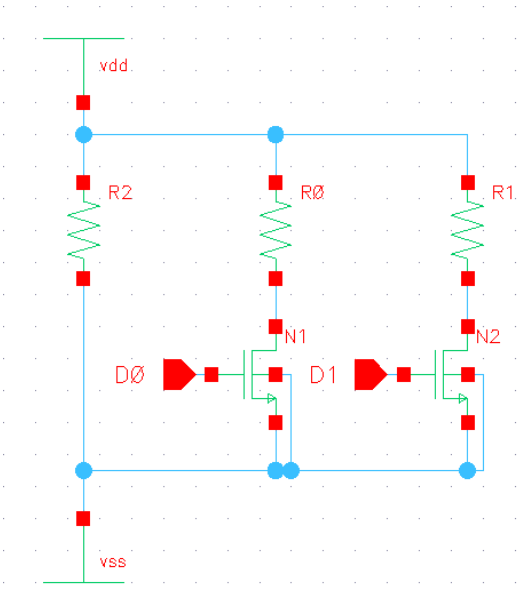



Figure 2.4.2

Another approach discussed was positioning the resistors in parallel which would result in the MOSFETS to be in series with the resistors. When a switch is open, current does not flow through the respective path; therefore, that path does not interact with the performance of the unit cell. When a switch is closed, current flows through the resistor which in turn will affect the performance of the unit cell. Unfortunately resistors in parallel are added by taking the inverse of the resistor value, so with a parallel resistor design the resistors become exponentially large. This negatively impacts the physical size of the design.

After looking at a series and parallel approach to trimming a resistor, the idea of combining them was approached. By combining the two designs previously discussed we hope to mitigate the negative effects each of the designs have. Figure 2.4.3 shows a matrix of resistors that have resistors in series and parallel. Then by using switches between the paths we are able to control the flow of current through the matrix of resistors. This then results in a trimmable resistor with the negative effects being mitigated in the process.

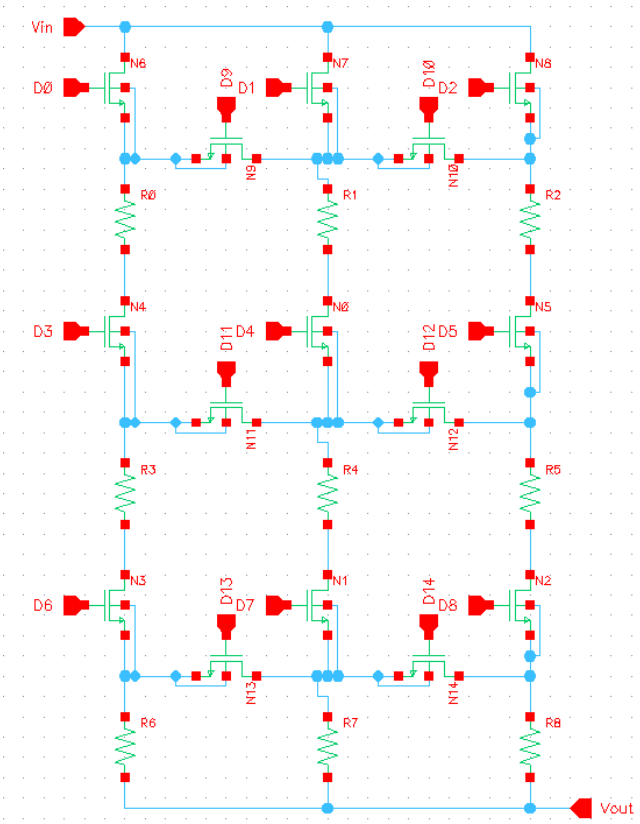



Figure 2.4.3

# 3. Statement of Work

## 3.1 Previous Work And Literature

One relevant work of literature for this project is the textbook Analog Integrated Circuit Design by T. C. Carusone, K. W. Martin, and D. Johnsby [2]. Another good resource on this topic is the book Microelectronic Circuits by A. S. Sedra and K. C. Smith [3].

The previous work of this type of trimming has been used in many applications requiring the ability to precisely trim a chip after manufacturing where laser trimming is not applicable. Documentation of previous work includes a patent by Cardiac Pacemakers Inc, where digitally trimmable resistors were used for bandgap voltage reference [4]. This method used a series resistor structure which has been simulated as one of our reference designs. This design has the shortcoming of having a poor temperature coefficient due to the large amount of current flowing through the switches.

Another popular method for trimmable resistors is the ladder structure. In a patent invented by Jimmy R. Naylor, a R/2R Ladder structure of resistors was implemented in order to create a new method for digital to analog converters[5]. This ladder structure is a promising resistor structure because of its improvement on both the series and parallel approaches. This is the primary structure that our project will be focusing on improving.

Other methods of trimmable resistors include the patent Dual thin film precision resistance trimming by STMicroelectronics Inc [6]. This design implements a heater on the IC that can precisely control the temperature of the resistors. This utilizes the temperature coefficient properties to modify the resistance values and achieve a fine resistor trim. A drawback of using an on-chip heater is the amount of space that will be required to do so. Space is part of the project requirement and therefore the heater is not something that can be utilized. It also takes a lot of power to use an on-chip heater, which is another drawback of this approach.

## 3.2 Technology Considerations

The project will rely heavily on MOSFET technology as switches in the trimmable resistor. Current MOSFET technologies do have a few weaknesses, however. The major one is the non-linearity performance due to temperature effects. If the switches were ideal, then the performance degradation caused by temperature effects would not be an issue. Unfortunately, these effects are a genuine issue throughout this project. There are a few solutions to this issue. One such solution is to limit the amount of current flowing through the MOSFET to reduce the

adverse effects. The tradeoff of doing this will be the need for more switches in the circuit. Solutions to the temperature effects could result in a tradeoff. The pros and cons of each solution will need evaluating to ensure that the solution is a valid one.

In addition, there will be a tradeoff with the physical size of the circuit and the accuracy. As a focus on accuracy becomes a dominant player in our design, the circuit will become much larger; therefore, our team will need to define what an acceptable physical size of the circuit is and then pack as much accuracy into the circuit given the circuit size limitation.

## 3.3 Task Decomposition

In order to successfully complete the digitally programmable trimmable resistor, our team broke up the project into multiple tasks.

1) Meet with our advisor to discuss technical goals, progress, and to make changes as needed.
2) Research existing designs and review our fundamentals.
3) Ideate and discuss ideas our team brainstormed.
4) Simulate reference design and acquire temperature coefficient.
5) Simulate our designs and compare them to the reference design performance.
6) Pick the most promising design based on performance characteristics and hone it into a finished product.
7) Prepare presentation and documentation.

Above are the tasks that will help our team stay on track to finishing the project.

## 3.4 Possible Risks And Risk Management

One major hindrance to the success of our project is access to the virtuoso software needed in order to design and simulate potential circuits. Some reasons that might make it difficult to access Virtuoso would be remote desktop issues, vpn issues and lab room closures. Additionally, there may be times when team members will have issues with their internet access.

Another roadblock that might come up is simulation issues due to novice knowledge on the proper way to perform simulations within Virtuoso. Our team is going to rely heavily on the simulation results to determine the performance of circuit designs, but if simulation issues present themselves, then our team will need to remove this road block before any more progress can be made.

Lastly, when it comes to circuit design, there are a lot of nuances and rules that need to be understood in order to successfully get a circuit to behave properly. During the project it might become more apparent that our team's knowledge on

the general operations and behavior of circuits might be lacking and therefore cause some issues.

## 3.5 Project Proposed Milestones and Evaluation Criteria

Over the course of our projects progress, there are a few milestones that will need to be hit. Below lists a few of the milestones that our team will work towards reaching.

1) Measure the temperature coefficient of a MOSFET.
2) Measure the temperature coefficient of a resistor.
3) Measure the temperature coefficient of a series trimmable resistor structure.
4) Pick one final circuit design to complete our project with.

By performing well established simulations, we should be able to confirm proper operation of the design. If there are any questions regarding the accuracy of any results, they can be directed to the faculty advisor. The faculty advisor is an expert in the area and should be able to provide us with meaningful and reliable guidance.

## 3.6 Project Tracking Procedures

We have decided to use Trello to keep track of progress and goals throughout the project. We are also utilizing Google Drive since we lack the knowledge of easy collaboration with Virtuoso. Google Drive allows us to share created content with other team members so that it can be improved upon.

## 3.7 Expected Results and Validation

The desired outcome is to design a digitally controllable trimmable resistor. This trimmable resistor will need to have high accuracy and low temperature dependencies in order to make it compete with current designs in the market.

For high level verification of the final design, our team will be using simulation environments in Virtuoso. The simulation results generated will be a direct reflection on the performance of the design.

# 4. Project Timeline, Estimated Resources, and Challenges

## 4.1 Project Timeline

sddec20-08 Gantt chart


The plan is to have the work split up between two semesters, using the first semester mostly for research, administration, and ideation. The first half should lay proper groundwork leading into the second half of the project. The focus in the second half will be choosing specific designs that show promise and refining them. The end goal will be to create a design that meets the project requirements. The focus will then shift to preparing documentation and running proper tests to confirm everything is accurate. Finally, we will present our findings to an industry panel along with the documentation that was developed, proving that the design meets the project requirements.

## 4.2 Feasibility Assessment

This project will consist of researching current methodologies of resistor trimming technologies. The goal will be to improve upon current technologies and develop a new resistor concept that garners interest as a useful product in the electronics community. In particular, the product will be a high-resolution digitally trimmable resistor that has no temperature dependencies. The challenges associated with this project are mostly that of the feasibility variety. It is not yet known if such a product can be developed. Research and development in this area requires specialization of the topic. Another challenge that could be encountered are simulation results that may not quite align with reality. Simulation results will also be subject to misinterpretation

## 4.3 Personnel Effort Requirements

| Task | Time/Person |
|---|---|
| Administrative | 30 hrs |
| Research | 60 hrs |
| Ideate | 30 hrs |
| Simulate | 40 hrs |
| Development | 80 hrs |
| Documentation/Presentation | 40 hrs |

### 4.4 Other Resource Requirements

The materials needed for this project are as follows:

- Computers for each team member
- Internet connection for each team member
- Communication software
- Simulation software

All of these materials are accessible by each member with no extra associated costs.

### 4.5 Financial Requirements

There are no anticipated financial resources required to conduct the project. Everything will be digitally designed and simulated. All resources for this have been provided by Iowa State University at no cost. There is a possibility for fabrication of the final design but that is not something that is anticipated at this current time.

# 5. Testing and Implementation

Testing is an **extremely** important component of most projects, whether it involves a circuit, a process, or a software library

Although the tooling is usually significantly different, the testing process is typically quite similar regardless of CprE, EE, or SE themed project:

1. Define the needed types of tests (unit testing for modules, integrity testing for interfaces, user-study for functional and non-functional requirements)
2. Define the individual items to be tested
3. Define, design, and develop the actual test cases
4. Determine the anticipated test results for each test case 5. Perform the actual tests
6. Evaluate the actual test results
7. Make the necessary changes to the product being tested 8. Perform any necessary retesting
9. Document the entire testing process and its results

Include Functional and Non-Functional Testing, Modeling and Simulations, challenges you've determined.

## 5.1 Interface Specifications

– Discuss any hardware/software interfacing that you are working on for testing your project

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## 5.2 Hardware and software

– Indicate any hardware and/or software used in the testing phase

– Provide brief, simple introductions for each to explain the usefulness of each

## 5.3 Functional Testing

Examples include unit, integration, system, acceptance testing

## 5.4 Non-Functional Testing

Testing for performance, security, usability, compatibility

## 5.5 Process

– Explain how each method indicated in Section 2 was tested

– Flow diagram of the process if applicable (should be for most projects)

## 5.6 Results

– List and explain any and all results obtained so far during the testing phase

- – Include failures and successes
- – Explain what you learned and how you are planning to change it as you progress with your project
- – If you are including figures, please include captions and cite it in the text

• This part will likely need to be refined in your 492 semester where the majority of the implementation and testing work will take place

-**Modeling and Simulation**: This could be logic analyzation, waveform outputs, block testing. 3D model renders, modeling graphs.

-List the **implementation Issues and Challenges**.

# 6. Closing Material

## 6.1 Conclusion

Summarize the work you have done so far.  Briefly re-iterate your goals. Then, re-iterate the best plan of action (or solution) to achieving your goals and indicate why this surpasses all other possible solutions tested.

## 6.2 References


[1]

[2] T. C. Carusone, K. W. Martin, and D. Johns, *Analog integrated circuit design, 2nd edition*. Hoboken, NJ: John Wiley & Sons, 2011.

[3] A. S. Sedra and K. C. Smith, *Microelectronic circuits*. New York: Oxford University Press, 2015.

[4]Cardiac Pacemakers, Inc., 2020. *Digitally Trimmable Resistor For Bandgap Voltage Reference*. US6381491B1.

[5]

[6]


This will likely be different than in project plan, since these will be technical references versus related work / market survey references. Do professional citation style(ex. IEEE).

## 6.3 Appendices

Any additional information that would be helpful to the evaluation of your design document.

If you have any large graphs, tables, or similar that does not directly pertain to the problem but helps support it, include that here. This would also be a good area to include hardware/software manuals used. May include CAD files, circuit schematics, layout etc. PCB testing issues etc. Software bugs etc.