Digitally Controlled Trimmable Resistor

DESIGN DOCUMENT

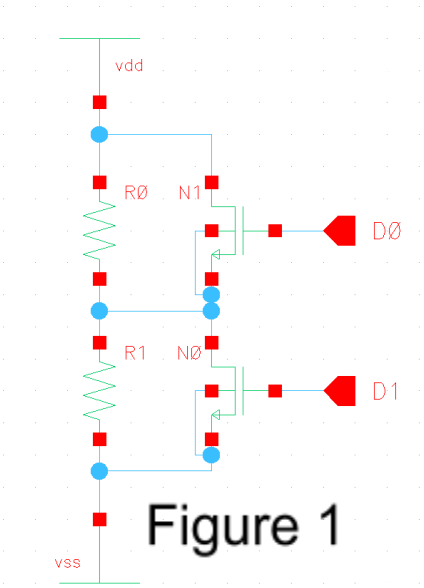

Figure 1

Team Number: 8

Client: Prof. Randy Geiger
Advisers: Prof. Randy Geiger

Team Members/Roles:
Clark Reimers - Test Engineer
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Revised: 02/22/2020

Executive Summary

Development Standards & Practices Used

- IEEE - Following all IEEE codes of ethics and designing standards for integrated circuits.
- Virtuoso - Follow all virtuoso rules when designing the circuit schematic, layout and running simulation.
- TSMC Process Parameters - To design our project in virtuoso given process parameters will be followed to make the circuit simulatable and manufacturable.
- Design Flow - Follow a design flow methodology presented in class in order to organize our projects progress. This includes Empathy, Define, Ideate, Prototype, and Test.

Summary of Requirements

- Make a device in .18u CMOS process with adjustable resistance
- Make the resistor highly accurate with a 1% trim
- Size the layout of the circuit to compete with trimmable resistors currently available
- Minimize temperature dependencies within the design
- Manage process variations issues within the design and layout of the circuit
- Be able to adjust the resistance with a discrete input

Applicable Courses from Iowa State University Curriculum

- EE 201 - This course provides the background on relevant passive components that will be used in our design. This also gives us some of the mathematical tools necessary to work with analyzing the passive components in our circuit.
- EE 230- This course covers operational amplifiers. These devices will be used in our simulations.
- EE 330- This course provides the background for our semiconductor devices inside of our IC. The most predominant devices of our design will be resistors and MOSFETs. This course also teaches us how to do physical layout of an IC.

- CPR E 281- This gives us the digital background for our digitally controlled trimmable resistor. Encoders, decoders, and other digital logic that we will use in our design was learned here.
- MATH 267- Differential equations gives us many analysis techniques that are applicable with circuitry. This course is a foundation for the development of our op-amps.
- EE 332- Physics of semiconductors. This course is extremely in depth into the characteristics of the materials used to create the switches (mosfets) used in this project design.
- LIB 160- This course provides a solid understanding of information literacy and the research process. Since most of our project is research, LIB 160 allowed us to discover many web resources for our research via the use of library discovery tools.
- EE 394- This course helped us to discover the importance of ethics in everything we do.
- ENGL 314- While making our way through this project, we will need to do a lot of documentation. English 314 taught us how to successfully communicate technical information to a specific target audience.

New Skills/Knowledge acquired that was not taught in courses

List all new skills/knowledge that your team acquired which was not part of your Iowa State curriculum in order to complete this project.

- Research - Although we discussed resources for research in LIB 160, we have not actually had any courses that focused on pure research.
- Website management- We are a group of mostly electrical engineers with the exception of one computer engineer. This being the case, we have not really dealt with using/designing/managing websites up until this point.
- Several tools and resources- We have learned about the existence of different tools and resources that have been helpful for our progress so far and will continue to be helpful down the road.

Table of Contents

List of figures/tables/symbols/definitions (This should be the similar to the project plan)

Definitions:

EE - electrical engineering

CPR E - computer engineering

IC- integrated circuit

MOSFET - metal oxide semiconductor field effect transistor

PCB - Printed Circuit Board

.18u CMOS process

Figures:

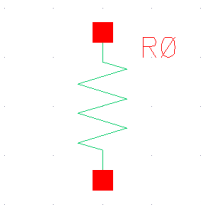
1 - Title Page Picture

2.4.1 - Series Resistor Design

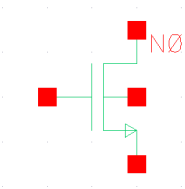
2.4.2 - Parallel Resistor Design

2.4.3 - Matrix Resistor Design

Symbols:



Resistor



NMOS transistor

1 Introduction

1.1 Acknowledgement

A big thanks to Randy Geiger for his technical advice throughout our project.

1.2 Problem and Project Statement

Currently in industry, there is a need to modify resistance values for a resistor that has been implemented into a working circuit design. There is a way to do this trimming with the use of laser cutting of the resistor film to finely set the desired resistance value. This has the disadvantage of being expensive as well as impossible to do once the IC has been packaged. Also, It is a one-time process that only allows the resistor to be trimmed once. Another solution is with a digital potentiometer using a series or parallel resistor structure. This solution has low-resolution trimming capabilities with either poor temperature coefficients or physically large components.

This project aims to create a high-resolution digitally trimmable resistor that will fix many of the current solutions to the need for trimmable resistors. This device will be able to set many different resistance values using a digital input that can be finely tuned to different resistor values within a set range. Focusing on improving the architecture based on resistors and switches, the goal is to construct a digitally trimmable resistor that has a high resolution with good temperature coefficients.

1.3 Operational Environment

There are no specific plans for the environment of our IC. Conditions such as dust and rain could be mitigated through a device enclosure. Since one of the goals is to minimize the temperature dependencies on the MOSFETs and resistors, extreme temperatures should also not be an issue. As such, the design can be utilized in most conditions.

1.4 Requirements

This device requires a resistor that can be repeatedly trimmed over many iterations. It should be able to modify the resistances by around 1% per step. This device will require the use of a decoder to set the digital inputs necessary to select a resistance value. It will require a pcb to house the device in order to resist

current. Another requirement for our project is that it minimizes temperature dependencies.

1.5 Intended Users and Uses

A digital trimmable resistor would be used in applications that require an initial calibration, it would allow certain parameters to be altered. An example of where a trimmable resistor would be used is a cardiac pacemaker, that would require the parameter to be changed when called upon.

1.6 Assumptions and Limitations

Assumptions: Resistors and MOSFET devices are temperature dependent by nature. There would be process variations, only resistors and mosfets switches would be used, should be able to be trimmed many times.

Limitations: The total value of resistor and size of the switch shouldn't be big. The trimming should be at a resolution of 1% per step. The temperature coefficient should be at or less than beta ppm/°C.

1.7 Expected End Product and Deliverables

For this project, the expected deliverable is a new method for a digitally trimmable resistor, as opposed to what is currently being used. The design will be within the limitations provided. After coming up with a new approach and the appropriate measurements, the circuit would be simulated using the .18u CMOS process. The end goal is to get a simulation of a device that will meet the constraints set by the client. No physical deliverable is required.

2. Specifications and Analysis

2.1 Proposed Approach

Current Progress:

A lot of the current progress has been doing research. In order to design a functional circuit that meets the constraints of the client, it is important that the components used are fully understood. The next step in the process is to look at patents for trimmable resistors to gain more insight. Research has uncovered some neat approaches to solving the problem for the task at hand and some important uses have been found for the approaches. After learning about some approaches that could be useful for our problem, initial designs have been drafted that could work to meet the end goal.

Approaches:

The initial approach was to build on basic understandings, develop some circuits, test, and revise. The approach has not been changed yet but may be done further down the road as new information is uncovered and can be applied to the design. The initial approaches are testing current resistor structures to examine the pros/cons of these designs. Afterwards the initial design is produced into the modeling software and tested in comparison to the test designs.

Standards:

Relevancy to standards falls heavily under the IEEE code of ethics. As research is conducted about current industry practice, credit will be given according to contributions in the design where applicable. Since the end goal is a simulated circuit, other standards are not anticipated as relevant to this project.

2.2 Design Analysis

Initial methods tested include the series resistor design, and the parallel resistor design. These approaches have been modeled in Virtuoso and tested in order to examine the trimming resolution and temperature coefficient properties. The series design has a major flaw due to the current path flowing through MOSFETs, when current flows through the MOSFET, temperature variables affect the performance. The parallel designs' flaw shows up in the physical size of the IC due to the resistors being in parallel.

2.3 Development Process

For this project a waterfall development process is being followed. A lot of time has been spent in the requirements phase to study the effects of different current solutions in industry and find what constraints that will be selected for our design. A lot of research has been done on simpler approaches to the resistor structure. Some of the test designs have been implemented into Cadence Virtuoso to be compared with the initial design. This can be used as a more in depth form of researching for the first design step. Multiple initial designs have been drafted at this time as potential approaches to a more concrete design. An initial design has been implemented into Virtuoso in order to compare our other designs to a base.

2.4 Conceptual Sketch

Our initial intuition for making a trimmable resistor is to put resistors in series out to the N, and then put switches in parallel to a respective resistor. Then with an encoder the gates on the switches can be set to high or low resulting in the switches opening or closing. When a switch is closed, a short beside the resistor will occur which essentially will allow current to not flow through the resistor. This then allows for trimming of the overall resistor unit cell. Unfortunately when driving current through a MOSFET temperature variations are introduced. This is a big performance issue due to it breaking the voltage divider ratio by introducing temperature dependencies.

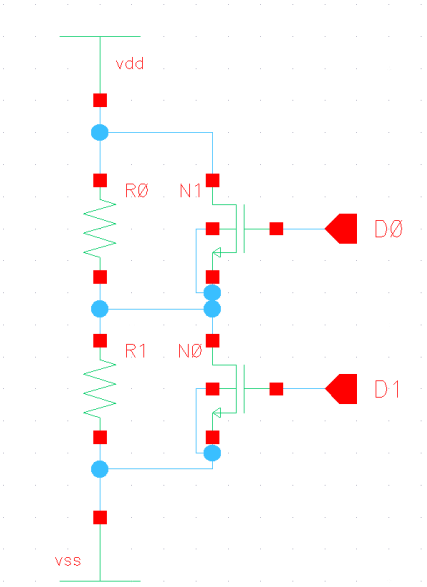


Figure 2.4.1

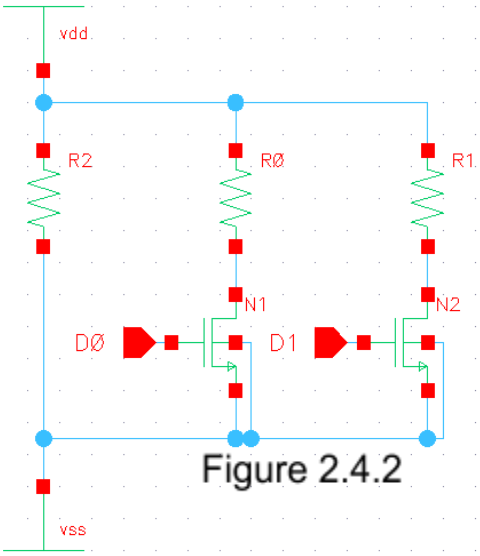


Figure 2.4.2

Another approach discussed was putting the resistors in parallel which would result in the MOSFETS to be in series with the resistors. When a switch is open, current does not flow through the respective path; therefore, that path does not interact with the performance of the unit cell. When a switch is closed, current flows through the resistor which in turn will affect the performance of the unit cell. Unfortunately resistors in parallel are added by taking the inverse of the resistor value, so with a parallel resistor design the resistors will grow exponentially large.

After looking at a series and parallel approach to trimming a resistor, we thought about combining them. By combining the two designs previously discussed we hope to mitigate the negative effects each of the designs have. Figure 2.4.3 shows a matrix of resistors that have resistors in series and parallel. Then by using switches between the paths we are able to control the flow of current through the matrix of resistors. This then results in a trimmable resistor hopefully with the negative effects being mitigated in the process.

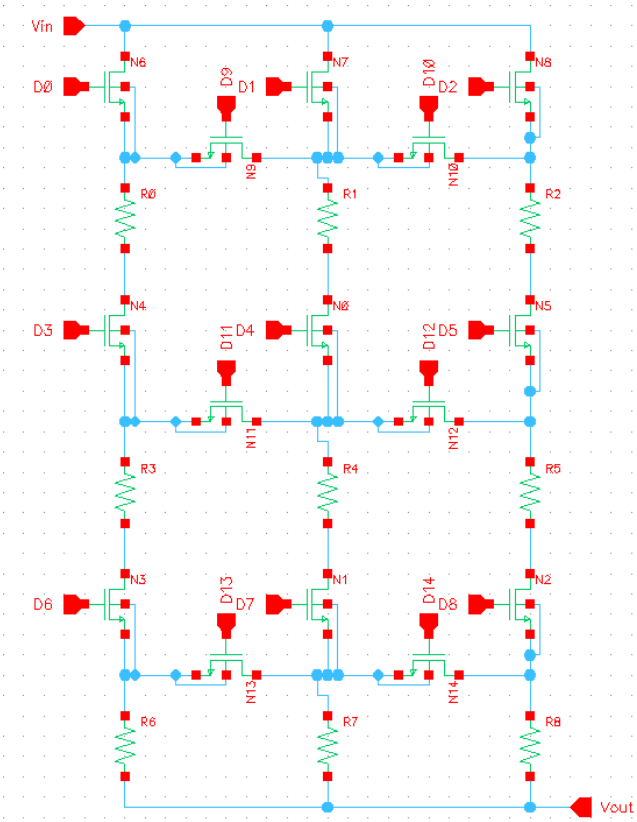


Figure 2.4.3

3. Statement of Work

3.1 Previous Work And Literature

Include relevant background/literature review for the project

– If similar products exist in the market, describe what has already been done

– If you are following previous work, cite that and discuss the **advantages/shortcomings**

– Note that while you are not expected to "compete" with other existing products / research groups, you should be able to differentiate your project from what is available

Detail any similar products or research done on this topic previously. Please cite your sources and include them in your references. All figures must be captioned and referenced in your text.

3.2 Technology Considerations

Highlight the strengths, weakness, and trade-offs made in technology available.

Discuss possible solutions and design alternatives

3.3 Task Decomposition

In order to solve the problem at hand, it helps to decompose it into multiple tasks and to understand interdependence among tasks.

3.4 Possible Risks And Risk Management

Include any concerns or details that may slow or hinder your plan as it is now. These may include anything to do with costs, materials, equipment, knowledge of area, accuracy issues, etc.

3.5 Project Proposed Milestones and Evaluation Criteria

What are some key milestones in your proposed project? Consider developing task-wise milestones. What tests will your group perform to confirm it works?

3.6 Project Tracking Procedures

What will your group use to track progress throughout the course of this and next semester?

3.7 Expected Results and Validation

What is the desired outcome?

How will you confirm that your solutions work at a **High level**?

4. Project Timeline, Estimated Resources, and Challenges

4.1 Project Timeline

• A realistic, well-planned schedule is an essential component of every well-planned project

• Most scheduling errors occur as the result of either not properly identifying all of the necessary activities (tasks and/or subtasks) or not properly estimating the amount of effort required to correctly complete the activity

• A detailed schedule is needed as a part of the plan:

– Start with a Gantt chart showing the tasks (that you developed in 3.3) and associated subtasks versus the proposed project calendar. The Gantt chart shall be referenced and summarized in the text.

– Annotate the Gantt chart with when each project deliverable will be delivered

• Completely compatible with an Agile development cycle if that's your thing

How would you plan for the project to be completed in two semesters? Represent with appropriate charts and tables or other means.

Make sure to include at least a couple paragraphs discussing the timeline and why it is being proposed. Include details that distinguish between design details for present project version and later stages of project.

4.2 Feasibility Assessment

Realistic projection of what the project will be. State foreseen challenges of the project.

4.3 Personnel Effort Requirements

Include a detailed estimate in the form of a table accompanied by a textual reference and explanation. This estimate shall be done on a task-by-task basis and should be based on the projected effort required to perform the task correctly and not just "X" hours per week for the number of weeks that the task is active

4.4 Other Resource Requirements

Identify the other resources aside from financial, such as parts and materials that are required to conduct the project.

4.5 Financial Requirements

If relevant, include the total financial resources required to conduct the project.

5. Testing and Implementation

Testing is an **extremely** important component of most projects, whether it involves a circuit, a process, or a software library

Although the tooling is usually significantly different, the testing process is typically quite similar regardless of CprE, EE, or SE themed project:

1. Define the needed types of tests (unit testing for modules, integrity testing for interfaces, user-study for functional and non-functional requirements)
2. Define the individual items to be tested
3. Define, design, and develop the actual test cases
4. Determine the anticipated test results for each test case 5. Perform the actual tests
6. Evaluate the actual test results
7. Make the necessary changes to the product being tested 8. Perform any necessary retesting
9. Document the entire testing process and its results

Include Functional and Non-Functional Testing, Modeling and Simulations, challenges you've determined.

5.1 Interface Specifications

– Discuss any hardware/software interfacing that you are working on for testing your project

5.2 Hardware and software

– Indicate any hardware and/or software used in the testing phase

– Provide brief, simple introductions for each to explain the usefulness of each

5.3 Functional Testing

Examples include unit, integration, system, acceptance testing

5.4 Non-Functional Testing

Testing for performance, security, usability, compatibility

5.5 Process

– Explain how each method indicated in Section 2 was tested

– Flow diagram of the process if applicable (should be for most projects)

5.6 Results

– List and explain any and all results obtained so far during the testing phase

- – Include failures and successes
- – Explain what you learned and how you are planning to change it as you progress with your project
- – If you are including figures, please include captions and cite it in the text

• This part will likely need to be refined in your 492 semester where the majority of the implementation and testing work will take place

-**Modeling and Simulation**: This could be logic analyzation, waveform outputs, block testing. 3D model renders, modeling graphs.

-List the **implementation Issues and Challenges**.

6. Closing Material

6.1 Conclusion

Summarize the work you have done so far. Briefly re-iterate your goals. Then, re-iterate the best plan of action (or solution) to achieving your goals and indicate why this surpasses all other possible solutions tested.

6.2 References

This will likely be different than in project plan, since these will be technical references versus related work / market survey references. Do professional citation style(ex. IEEE).

6.3 Appendices

Any additional information that would be helpful to the evaluation of your design document.

If you have any large graphs, tables, or similar that does not directly pertain to the problem but helps support it, include that here. This would also be a good area to include hardware/software manuals used. May include CAD files, circuit schematics, layout etc. PCB testing issues etc. Software bugs etc.